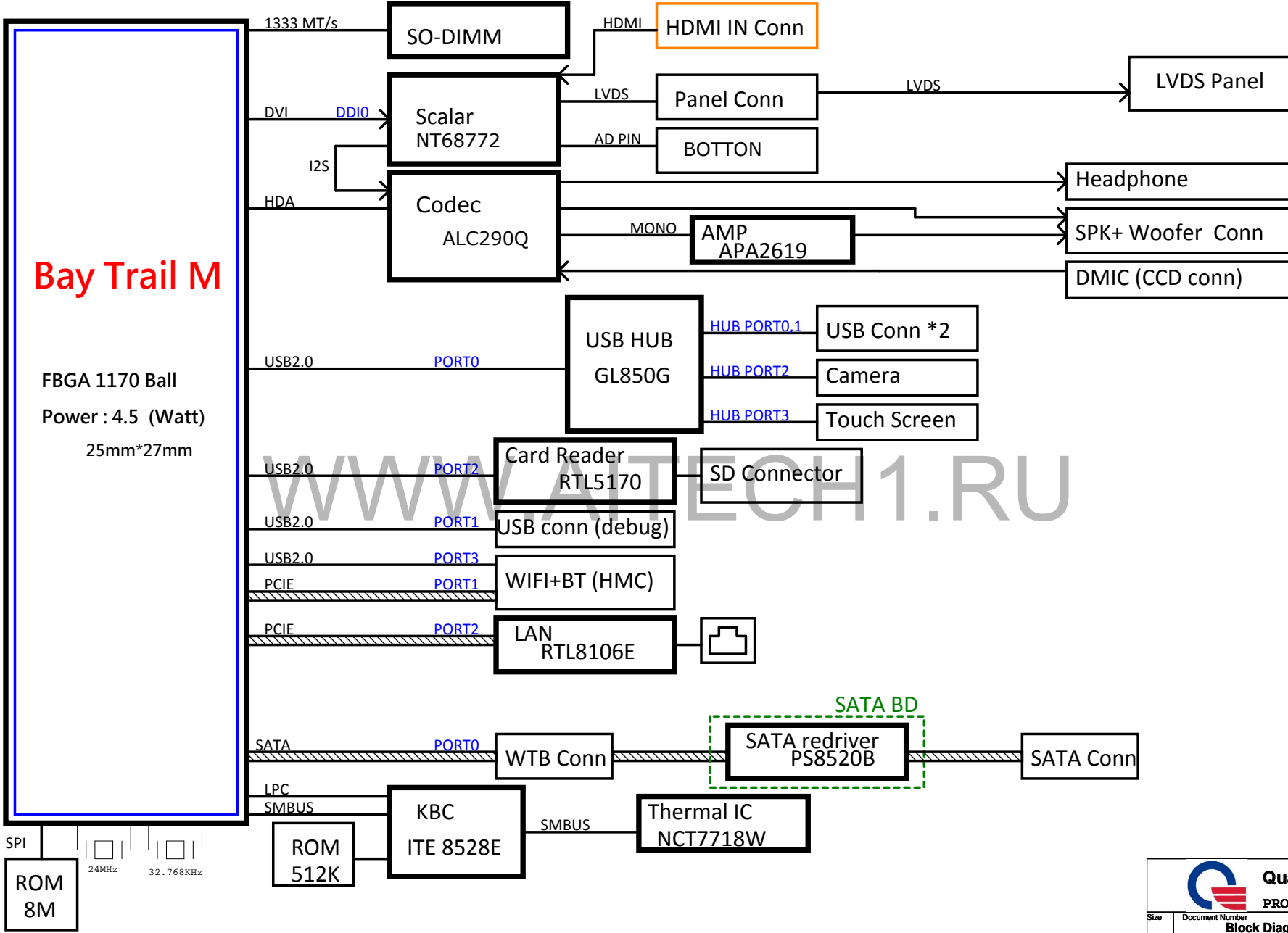


Foxglove BLOCK DIAGRAM



USB 2.0	Port Assignment
USBP0	USB HUB
USBP1	USB CONN
USBP2	CARDREADER
USBP3	BT

PCIE Master	Port Assignment
PCIE 0	WLAN/BT
PCIE 1	LAN
PCIE 2	(NC)
PCIE 3	(NC)


SATA Master	Port Assignment
SATA0	HDD
SATA1	NC

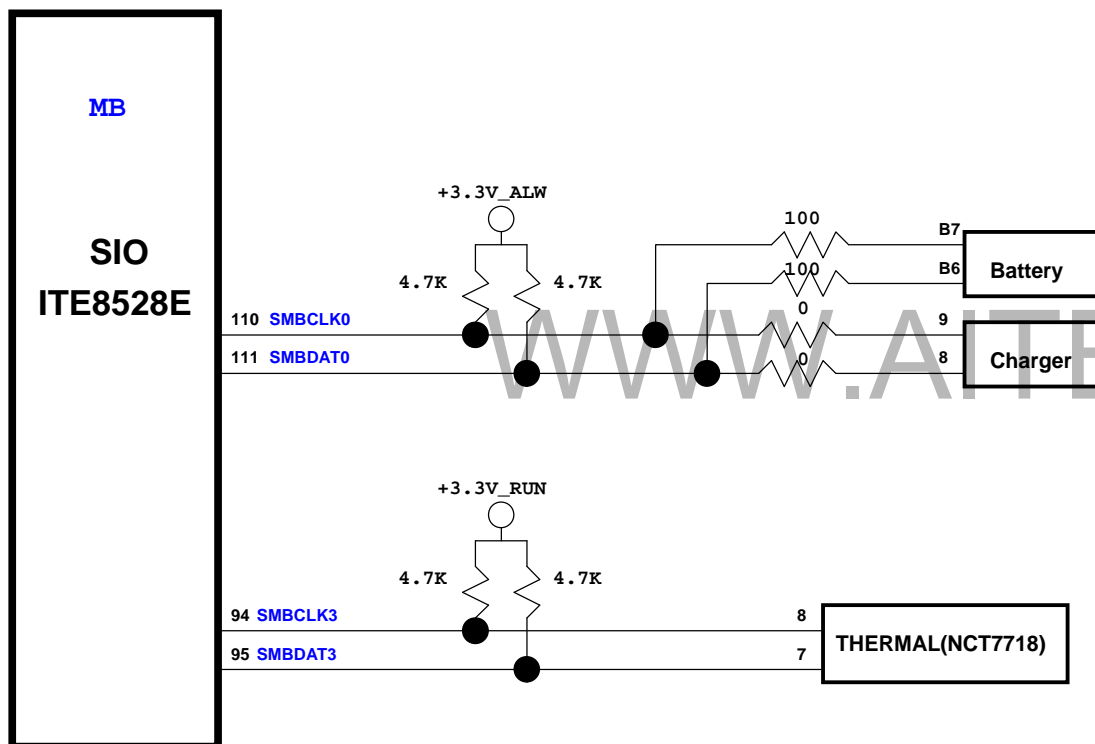
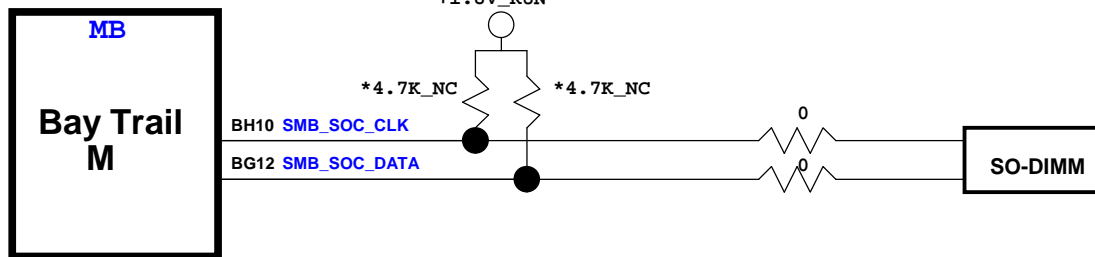
USB 3.0	Port Assignment
USBP0	NC

Display Port	Port Assignment
DDI0	DVI
DDI1	NC

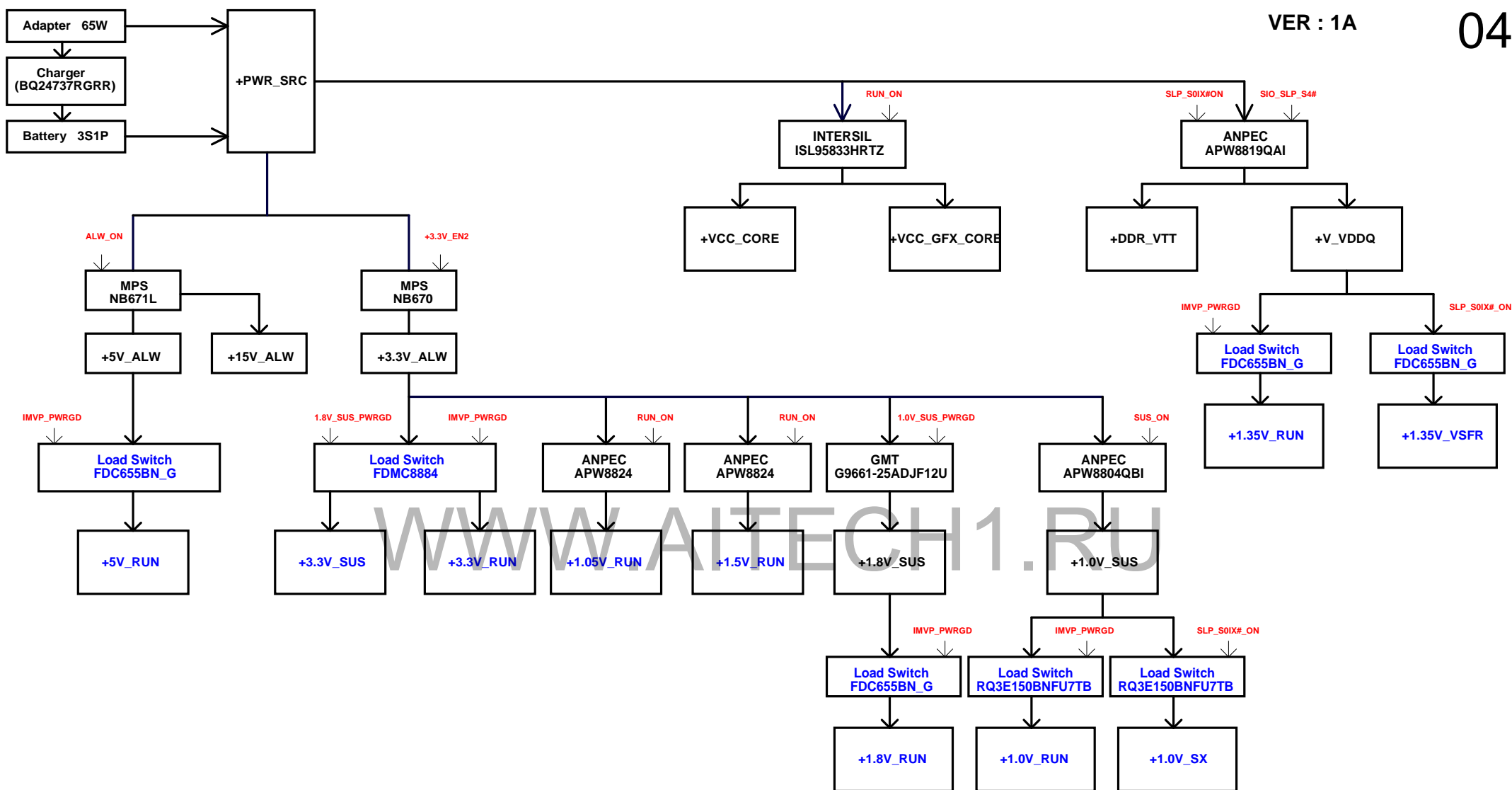
USB HUB	Port Assignment
USBP1	Touch Screen
USBP2	Camera Front
USBP3	Connector 1
USBP4	Connector 1

WWW.AITECH1.RU

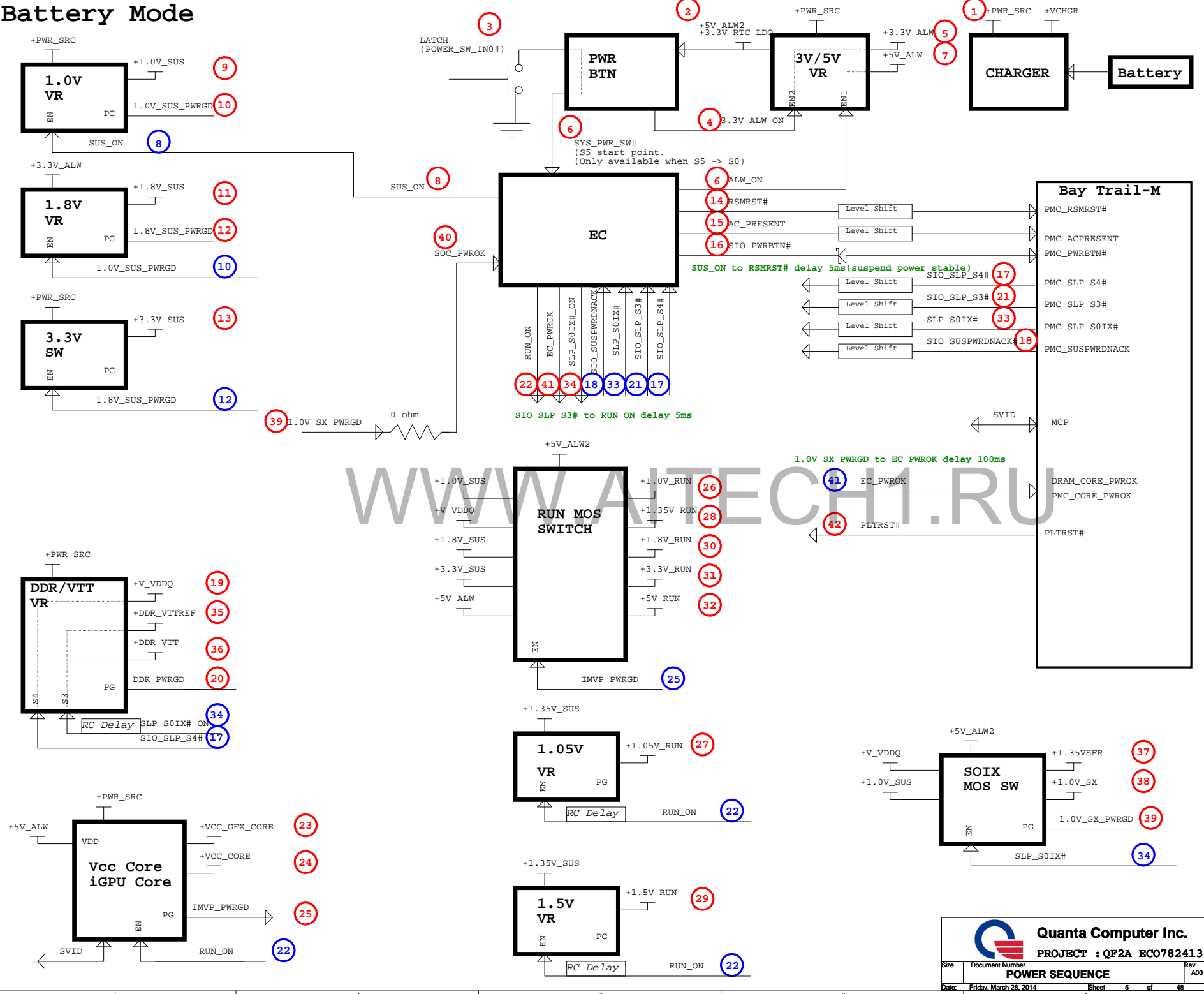
 Quanta Computer Inc. PROJECT : QF2A ECO782413		Rev A00
Date: Friday, March 28, 2014		Sheet 2 of 48



	Function	IC	Address
SMBUS	Thermal IC	NCT7718	1001100xb (98h)
	Charge IC	BQ24737RGRR	00010010 (0x12h)
	Battery	Battery	00010110 (0x16h)

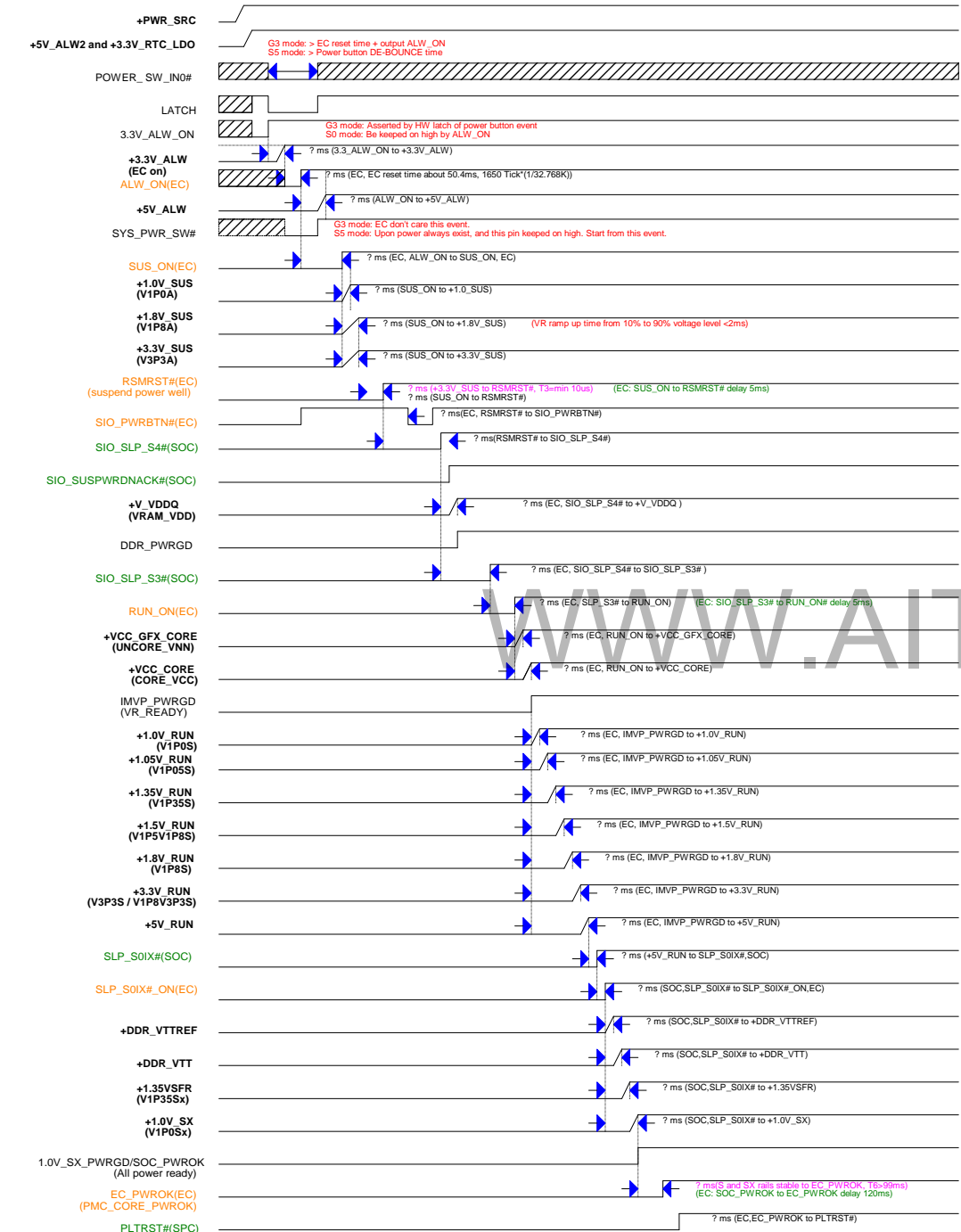


Battery Mode



ZM6 Power Sequence (G3 to S0)

Bay Trail-M EDS 512177, Rev1.2



G3

S0

DRAM: VIP35U (+V_VDDQ_VR)

U5A

[19] M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14 M_A_A15

[19] M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7

[19] M_A_RAS# M_A_CAS# M_A_WE#

[19] M_A_BS0 M_A_BS1 M_A_BS2

[19] M_A_CS#0 M_A_CS#1

[19] M_A_CKE0 M_A_CKE1

[19] M_A_ODT0 M_A_ODT2

[19] M_A_CLKP0 M_A_CLKN0

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

[19] M_A_CLKP1 M_A_CLKN1

DRAM0_MA_00 DRAM0_MA_11 DRAM0_MA_22 DRAM0_MA_33 DRAM0_MA_44 DRAM0_MA_55 DRAM0_MA_66 DRAM0_MA_77 DRAM0_MA_88 DRAM0_MA_99 DRAM0_MA_1010 DRAM0_MA_1111 DRAM0_MA_1212 DRAM0_MA_1313 DRAM0_MA_1414 DRAM0_MA_1515

DRAM0_DM_00 DRAM0_DM_11 DRAM0_DM_22 DRAM0_DM_33 DRAM0_DM_44 DRAM0_DM_55 DRAM0_DM_66 DRAM0_DM_77

DRAM0_RAS DRAM0_CAS DRAM0_WE

DRAM0_BS_00 DRAM0_BS_11 DRAM0_BS_22

DRAM0_CS_0 DRAM0_CS_2

DRAM0_CKE_00 DRAM0_CKE_22

DRAM0_ODT_0 DRAM0_ODT_2

DRAM0_CKP_0 DRAM0_CKN_0

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_CKP_2 DRAM0_CKN_2

DRAM0_DQ_00 DRAM0_DQ_11 DRAM0_DQ_22 DRAM0_DQ_33 DRAM0_DQ_44 DRAM0_DQ_55 DRAM0_DQ_66 DRAM0_DQ_77 DRAM0_DQ_88 DRAM0_DQ_99 DRAM0_DQ_1010 DRAM0_DQ_1111 DRAM0_DQ_1212 DRAM0_DQ_1313 DRAM0_DQ_1414 DRAM0_DQ_1515

DRAM0_DQ_1616 DRAM0_DQ_1717 DRAM0_DQ_1818 DRAM0_DQ_1919 DRAM0_DQ_2020 DRAM0_DQ_2121 DRAM0_DQ_2222 DRAM0_DQ_2323 DRAM0_DQ_2424 DRAM0_DQ_2525 DRAM0_DQ_2626 DRAM0_DQ_2727 DRAM0_DQ_2828 DRAM0_DQ_2929 DRAM0_DQ_3030 DRAM0_DQ_3131 DRAM0_DQ_3232 DRAM0_DQ_3333 DRAM0_DQ_3434 DRAM0_DQ_3535 DRAM0_DQ_3636 DRAM0_DQ_3737 DRAM0_DQ_3838 DRAM0_DQ_3939 DRAM0_DQ_4040 DRAM0_DQ_4141 DRAM0_DQ_4242 DRAM0_DQ_4343 DRAM0_DQ_4444 DRAM0_DQ_4545 DRAM0_DQ_4646 DRAM0_DQ_4747 DRAM0_DQ_4848 DRAM0_DQ_4949 DRAM0_DQ_5050 DRAM0_DQ_5151 DRAM0_DQ_5252 DRAM0_DQ_5353 DRAM0_DQ_5454 DRAM0_DQ_5555 DRAM0_DQ_5656 DRAM0_DQ_5757 DRAM0_DQ_5858 DRAM0_DQ_5959 DRAM0_DQ_6060 DRAM0_DQ_6161 DRAM0_DQ_6262 DRAM0_DQ_6363

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

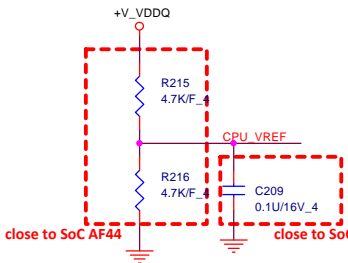
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DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

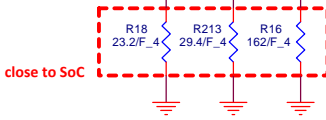
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DRAM0_DQSP_00 DRAM0_DQSN_00 DRAM0_DQSP_11 DRAM0_DQSN_11 DRAM0_DQSP_22 DRAM0_DQSN_22 DRAM0_DQSP_33 DRAM0_DQSN_33 DRAM0_DQSP_44 DRAM0_DQSN_44 DRAM0_DQSP_55 DRAM0_DQSN_55 DRAM0_DQSP_66 DRAM0_DQSN_66 DRAM0_DQSP_77 DRAM0_DQSN_77

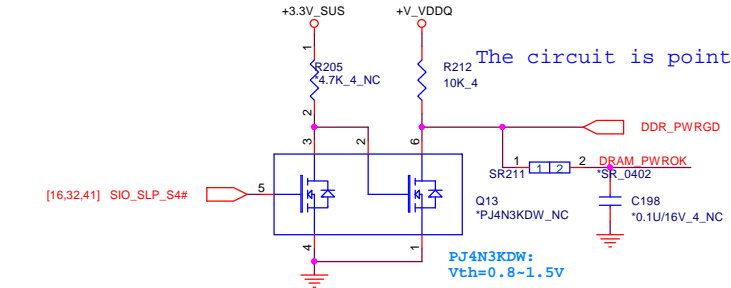


#add for SO-DIM

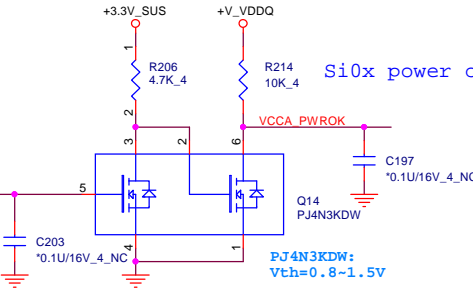
The DRAM_RCOMP[2:0] signals should be referenced to either Vss or Vdd planes (avoid referencing to noisy planes)



The circuit is pointless.



[11,32,36] EC_PWROK



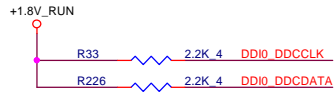
SiOx power ok ,Dram_core_pwrok high.

USB		
AY45	DRAM1_MA_00	DRAM1_DQ_00
BB47	DRAM1_MA_11	DRAM1_DQ_11
AW41	DRAM1_MA_22	DRAM1_DQ_22
BB44	DRAM1_MA_33	DRAM1_DQ_33
BB50	DRAM1_MA_44	DRAM1_DQ_44
BC53	DRAM1_MA_55	DRAM1_DQ_55
BB49	DRAM1_MA_66	DRAM1_DQ_66
BF50	DRAM1_MA_77	DRAM1_DQ_77
BC52	DRAM1_MA_88	DRAM1_DQ_88
BE52	DRAM1_MA_99	DRAM1_DQ_99
AY48	DRAM1_MA_1010	DRAM1_DQ_1010
BE51	DRAM1_MA_1111	DRAM1_DQ_1111
BD47	DRAM1_MA_1212	DRAM1_DQ_1212
BA51	DRAM1_MA_1313	DRAM1_DQ_1313
BH49	DRAM1_MA_1414	DRAM1_DQ_1414
BH50	DRAM1_MA_1515	DRAM1_DQ_1515
		DRAM1_DQ_1616
BD38	DRAM1_DM_00	DRAM1_DQ_1717
BH36	DRAM1_DM_11	DRAM1_DQ_1818
BC36	DRAM1_DM_22	DRAM1_DQ_1919
BH42	DRAM1_DM_33	DRAM1_DQ_2020
AT51	DRAM1_DM_44	DRAM1_DQ_2121
AM42	DRAM1_DM_55	DRAM1_DQ_2222
AK50	DRAM1_DM_66	DRAM1_DQ_2323
AK52	DRAM1_DM_77	DRAM1_DQ_2424
		DRAM1_DQ_2525
AV45	DRAM1_RAS	DRAM1_DQ_2626
AV44	DRAM1_CAS	DRAM1_DQ_2727
BB51	DRAM1_WE	DRAM1_DQ_2828
		DRAM1_DQ_2929
AY47	DRAM1_BS_00	DRAM1_DQ_3030
AY44	DRAM1_BS_11	DRAM1_DQ_3131
BF52	DRAM1_BS_22	DRAM1_DQ_3232
		DRAM1_DQ_3333
AT44	DRAM1_CS_0	DRAM1_DQ_3434
		DRAM1_DQ_3535
AT45	DRAM1_CS_2	DRAM1_DQ_3636
		DRAM1_DQ_3737
BG47	DRAM1_CKE_00	DRAM1_DQ_3838
BE46	RESERVED_BE46	DRAM1_DQ_3939
BD44	DRAM1_CKE_22	DRAM1_DQ_4040
BF48	RESERVED_BF48	DRAM1_DQ_4141
		DRAM1_DQ_4242
AP41	DRAM1_ODT_0	DRAM1_DQ_4343
AT42	DRAM1_ODT_2	DRAM1_DQ_4444
		DRAM1_DQ_4545
AV50	DRAM1_CKP_0	DRAM1_DQ_4646
AV48	DRAM1_CKN_0	DRAM1_DQ_4747
		DRAM1_DQ_4848
		DRAM1_DQ_4949
		DRAM1_DQ_5050
		DRAM1_DQ_5151
AT50	DRAM1_CKP_2	DRAM1_DQ_5252
AT48	DRAM1_CKN_2	DRAM1_DQ_5353
		DRAM1_DQ_5454
		DRAM1_DQ_5555
		DRAM1_DQ_5656
		DRAM1_DQ_5757
AT41	DRAM1_DRAMRST	DRAM1_DQ_5858
		DRAM1_DQ_5959
		DRAM1_DQ_6060
		DRAM1_DQ_6161
		DRAM1_DQ_6262
		DRAM1_DQ_6363
		DRAM1_DQSP_00
		DRAM1_DQSN_00
		DRAM1_DQSP_11
		DRAM1_DQSN_11
		DRAM1_DQSP_22
		DRAM1_DQSN_22
		DRAM1_DQSP_33
		DRAM1_DQSN_33
		DRAM1_DQSP_44
		DRAM1_DQSN_44
		DRAM1_DQSP_55
		DRAM1_DQSN_55
		DRAM1_DQSP_66
		DRAM1_DQSN_66
		DRAM1_DQSP_77
		DRAM1_DQSN_77

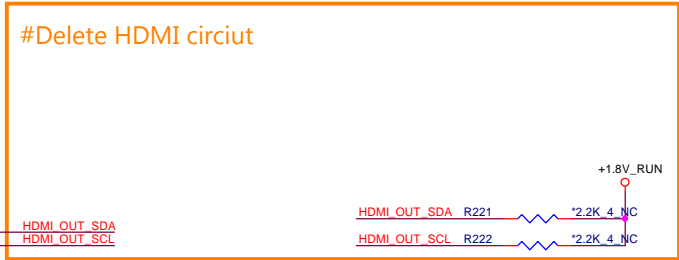
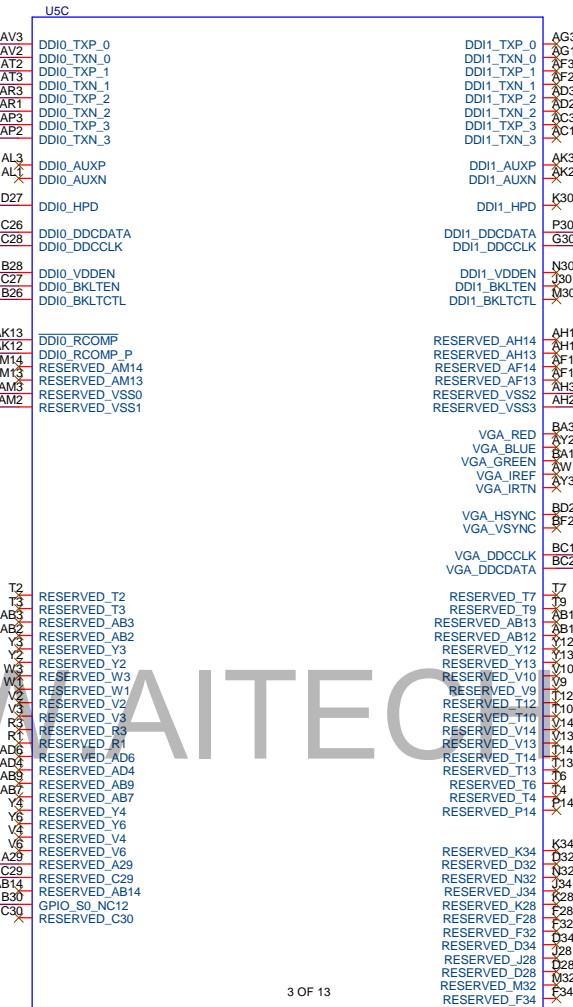
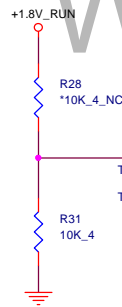
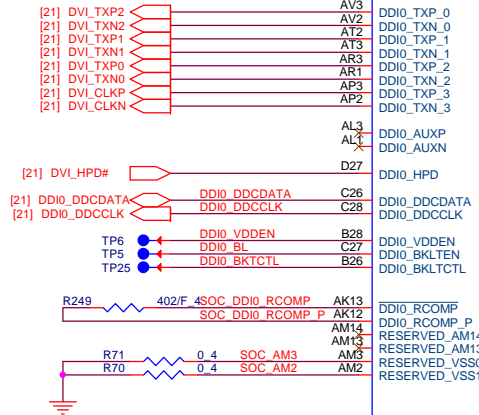
VLV_M_D/BGA
REV = 2.0

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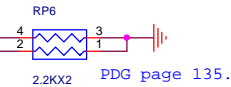
DDI_x TX/AUX: V1P0S_x (+1.0V_SX)
DDI_x HPD/DDC/VDDEN/BKLT: V1P8S (+1.8V_RUN)



HW Strap:DDI0 Detect	
DDI0_DDCDATA	
PU	1 = DDI0 detected
PD	0 = DDI0 not detected(Default)



HW Strap:DDI1 Detect	
DDI1_DDCDATA	
PU	1 = DDI1 detected
PD	0 = DDI1 not detected(Default)



PDG page 135.

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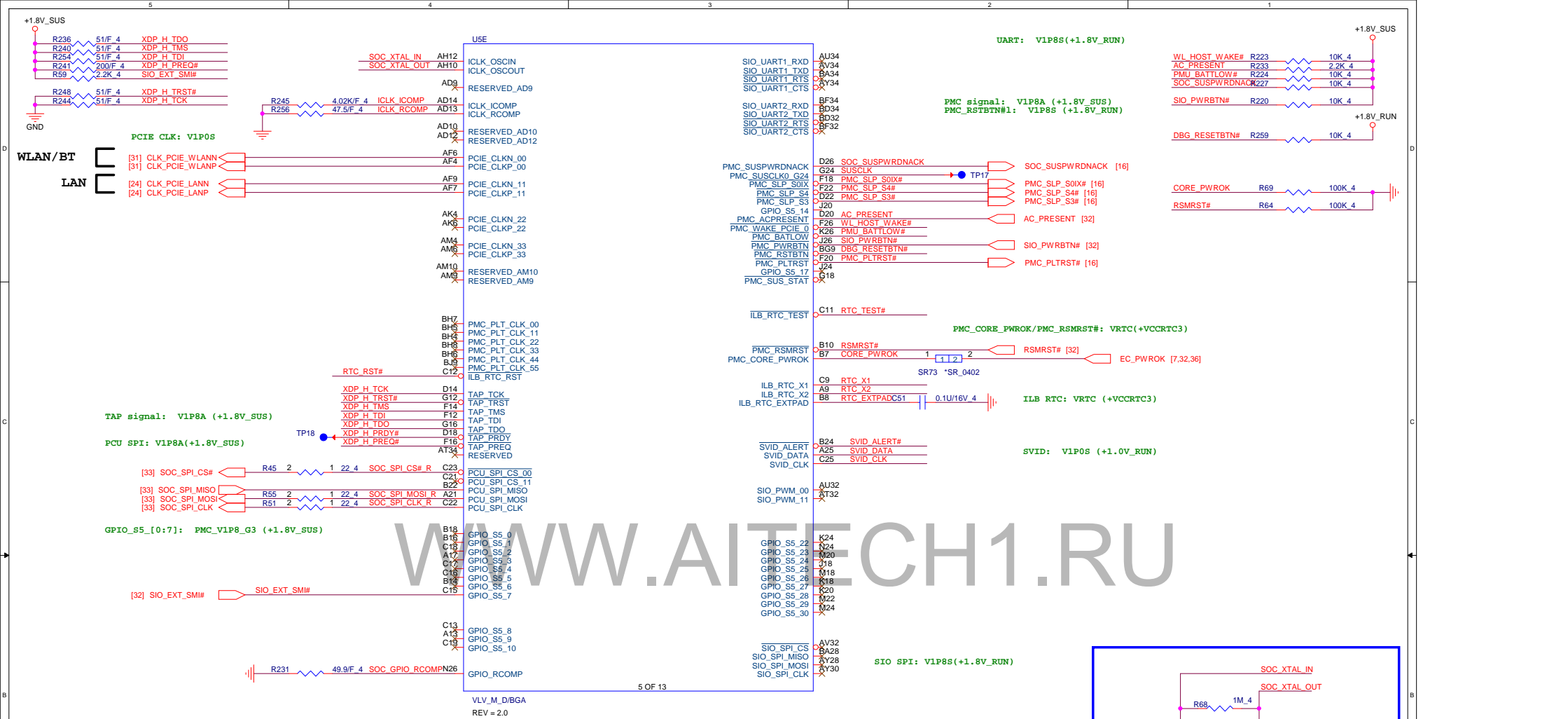
VLV_M_D/BGA
REV = 2.0



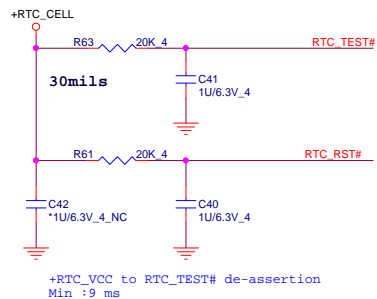
Quanta Computer Inc.

PROJECT : QF2A ECO782413

Size	Document Number	Rev
	Bay Trail M (DISPLAY)	A00
Date:	Friday, March 28, 2014	Sheet 9 of 48



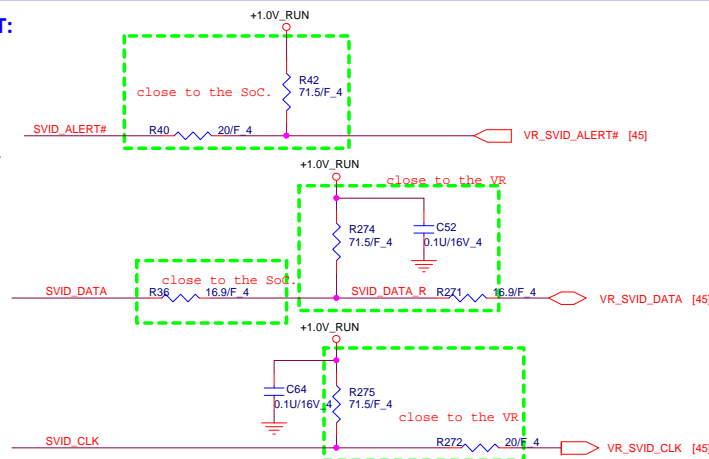
RTC Circuitry (RTC) (non Rechargeable BATT)



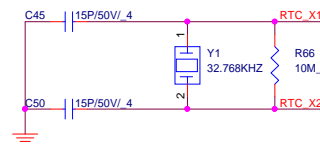
SVID_ALERT:

SVID_DATA

SVID_CLK



RTC Clock 32.768KHz

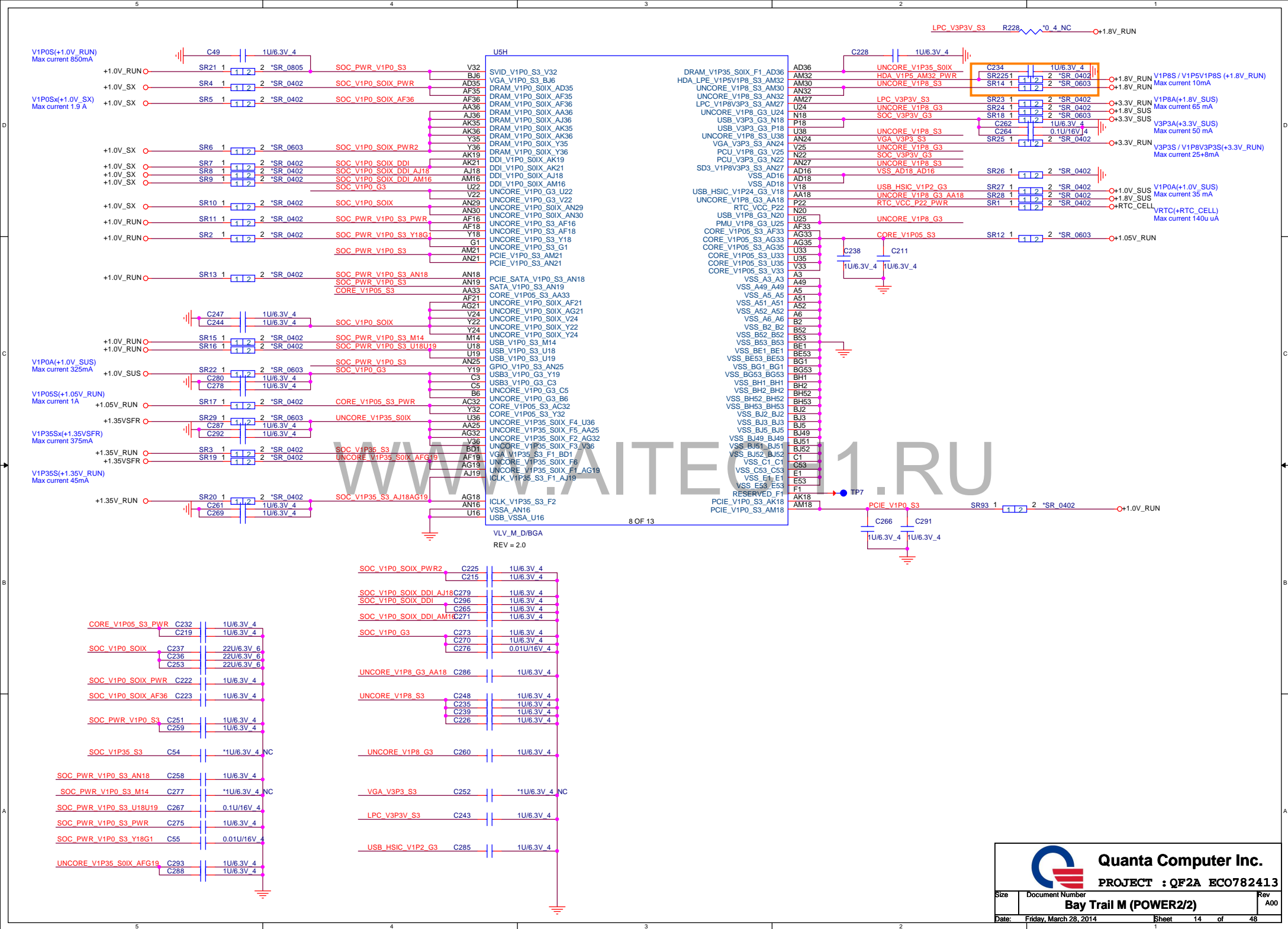


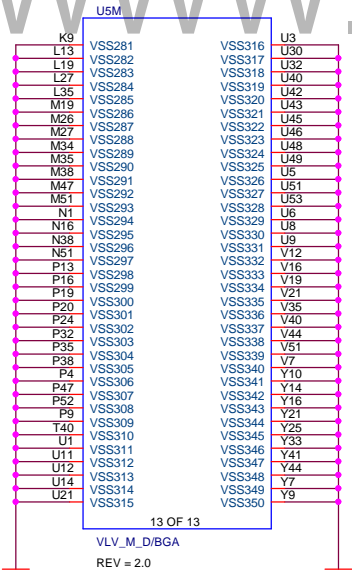
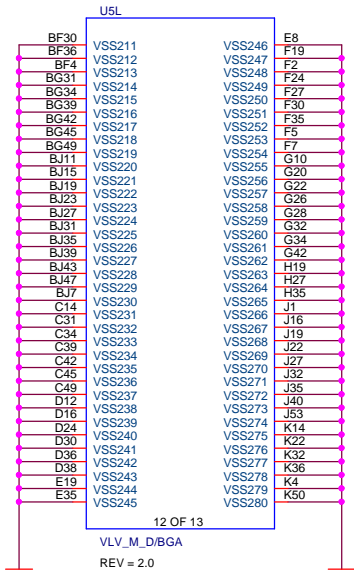
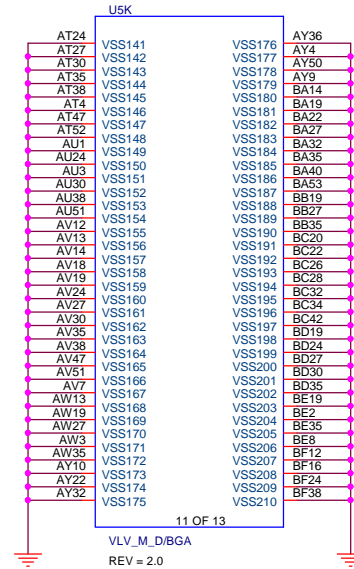
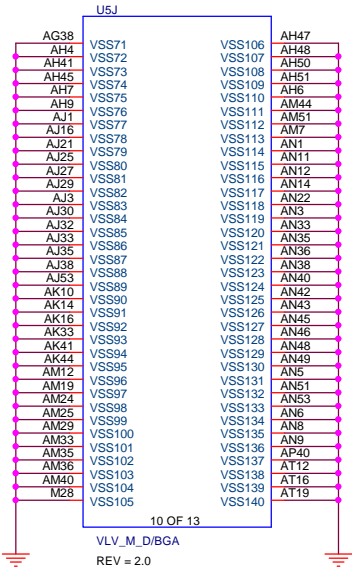
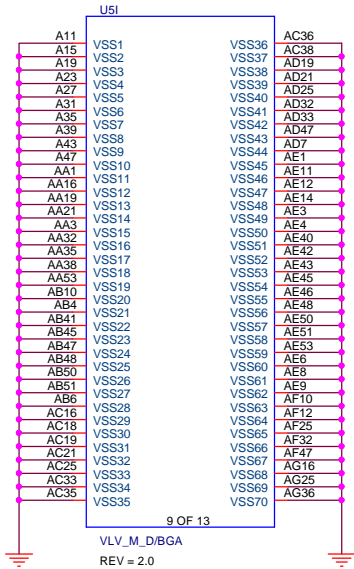
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Bay Trail M (CLK&PMC)

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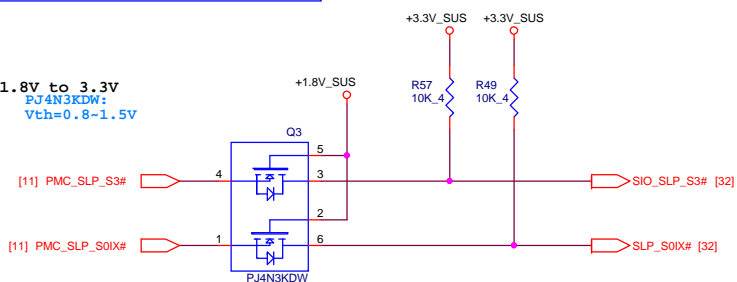




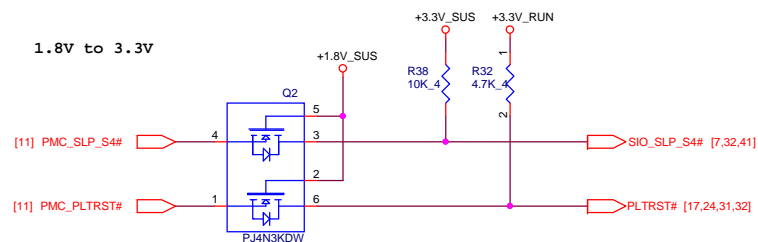
WWW.AITECH1.RU

Co-layout:
If mount R736, R744, need NC R511, R512, Q37

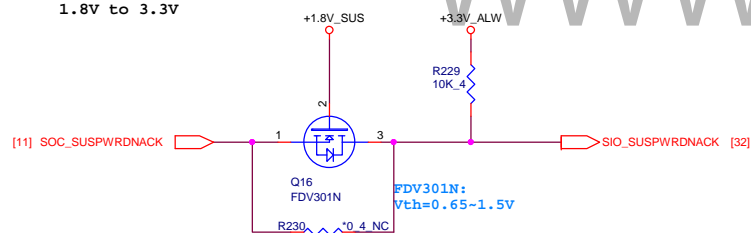
1.8V to 3.3V
PJ4N3KDW:
Vth=0.8-1.5V



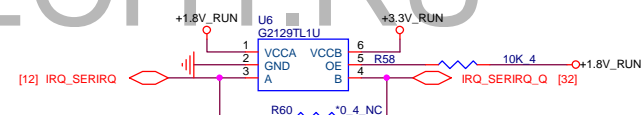
1.8V to 3.3V



1.8V to 3.3V

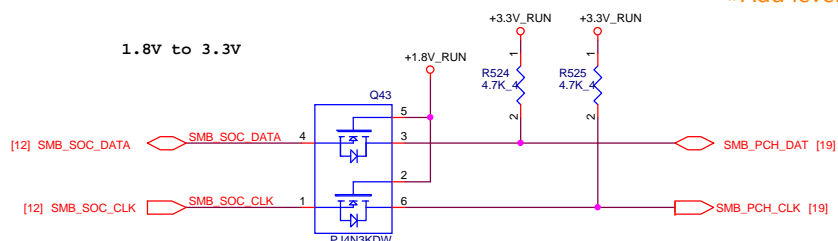


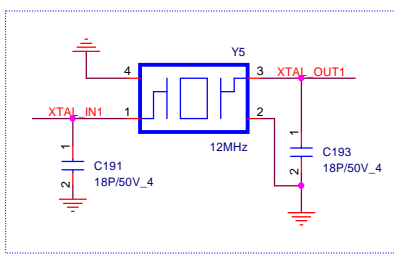
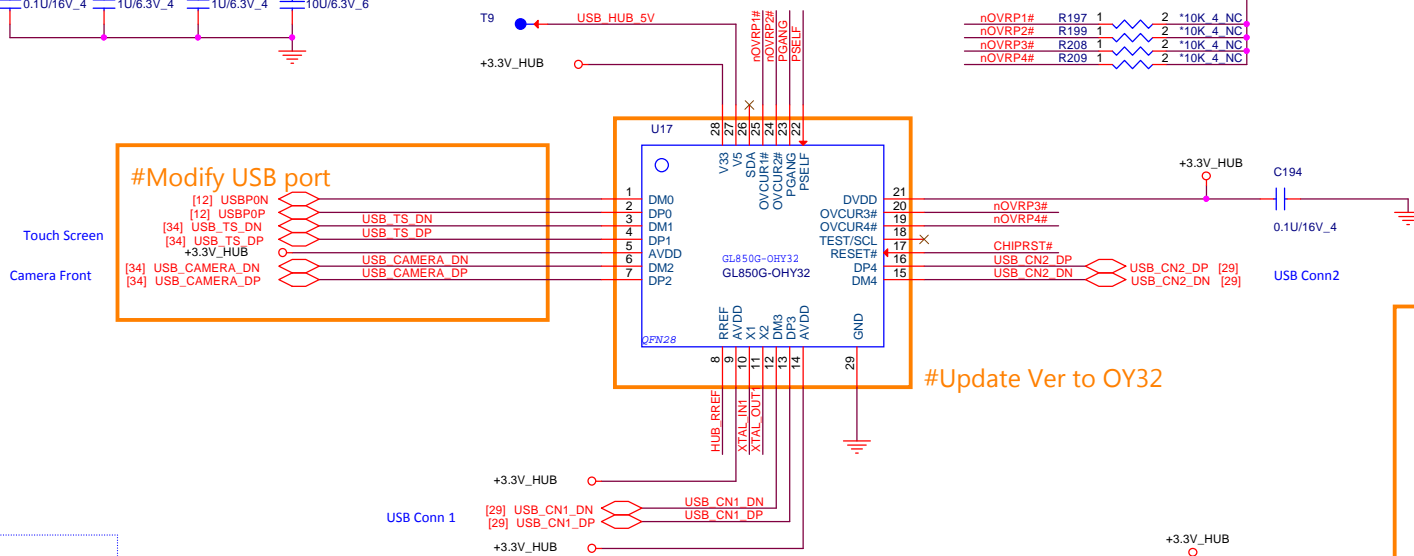
Co-layout:
If mount 0 ohm, need NC G2128TL1U and 10K.



#Add level shift for SO-DIMM

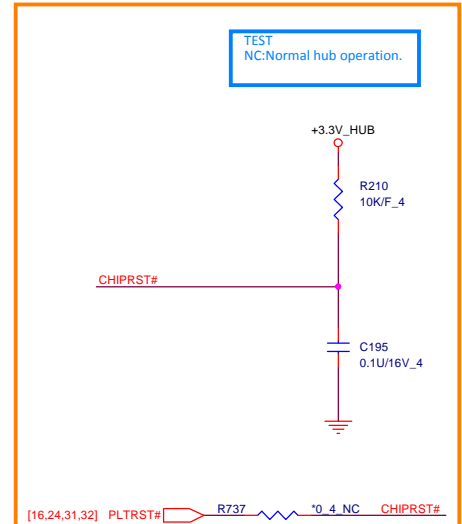
1.8V to 3.3V





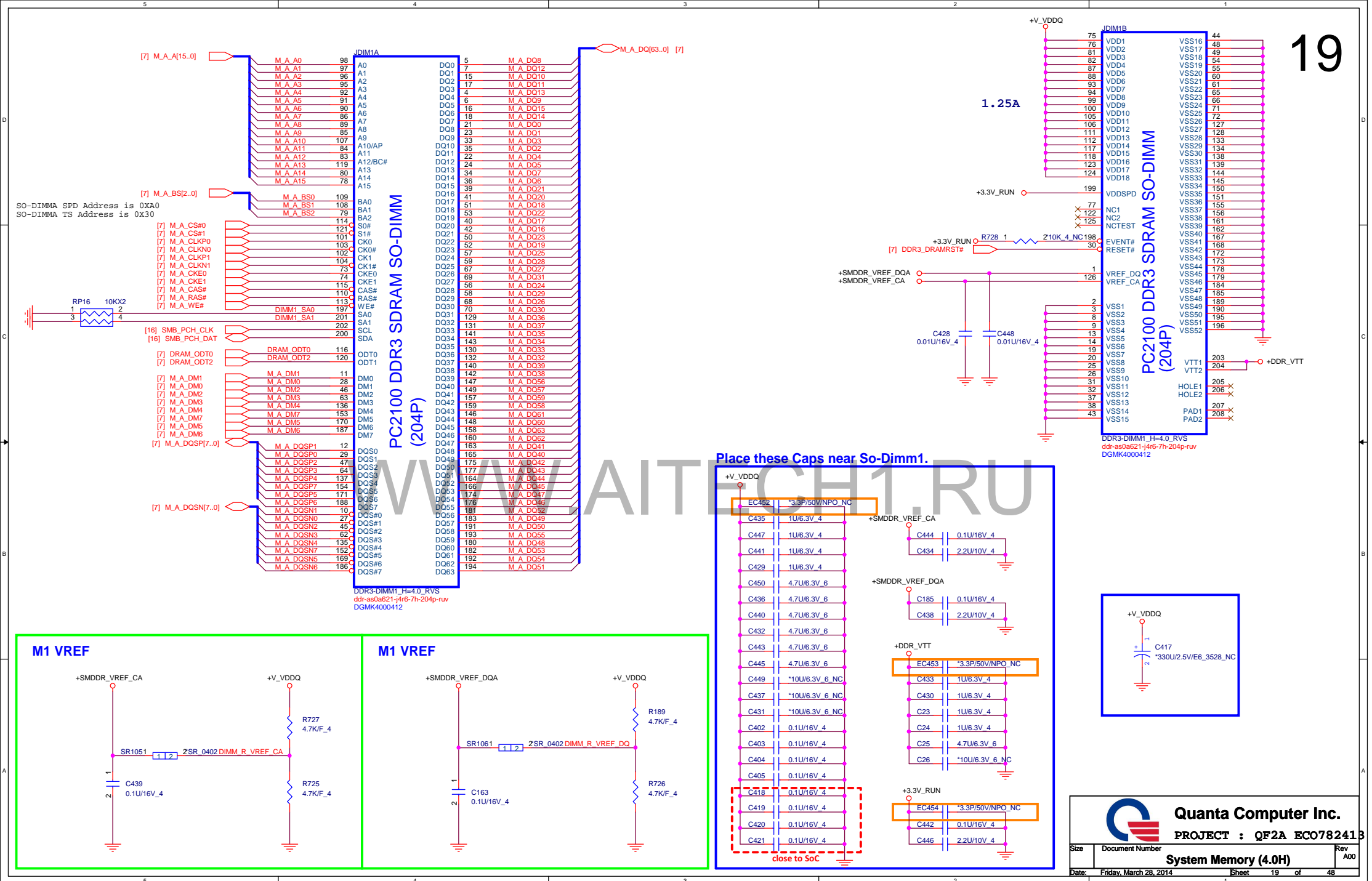
WWW.AITECH1.RU

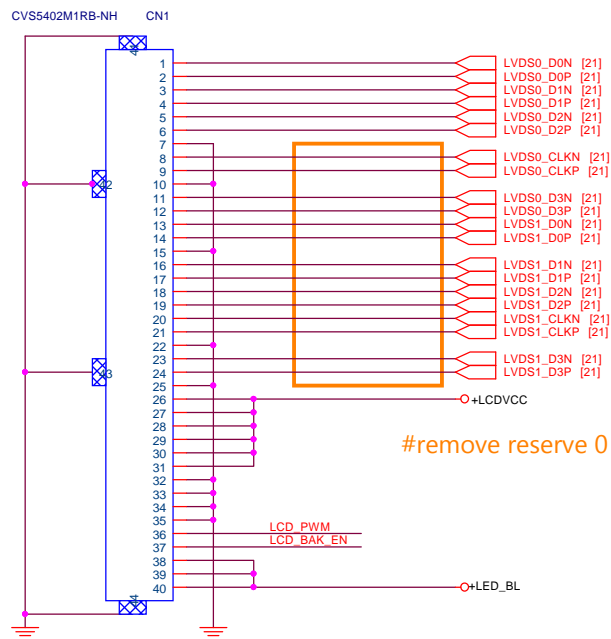
PGANG		PSELF		nOVRPx	
H	Gang mode	H	Power Self	Floating	Non-removable
L	Individual mode	L	Power Bus	Pull high	Removable



#Delete USB switch

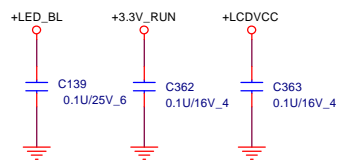
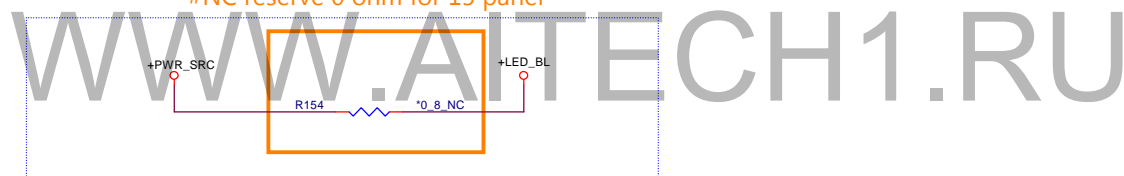
WWW.AITECH1.RU





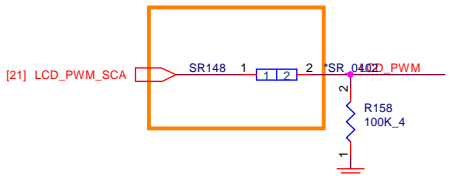
#remove reserve 0 ohm for 19" panel

#NC reserve 0 ohm for 15 panel

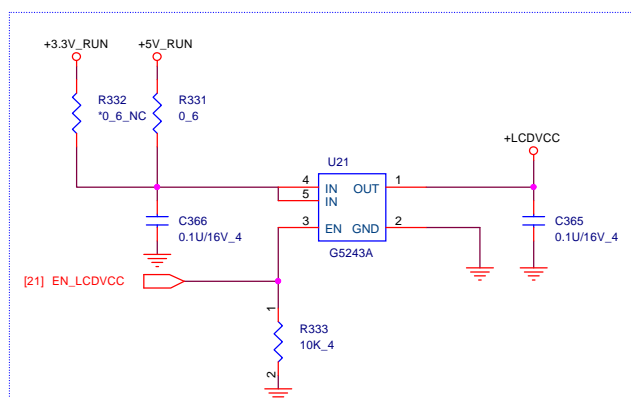
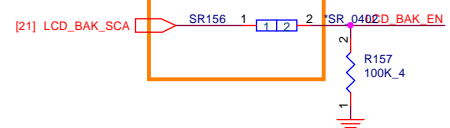


Close LCD connector

Brightness Control



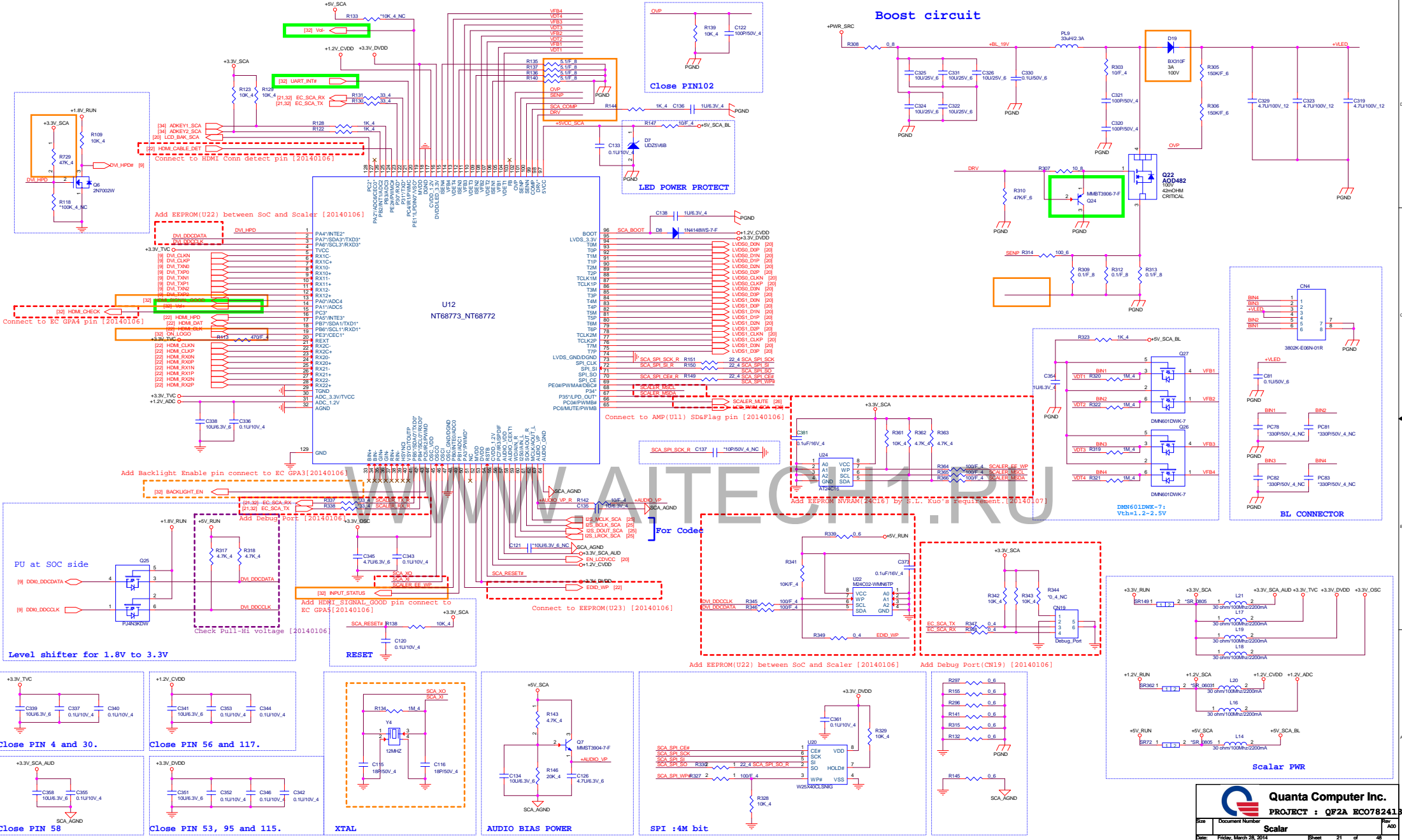
BAK_EN

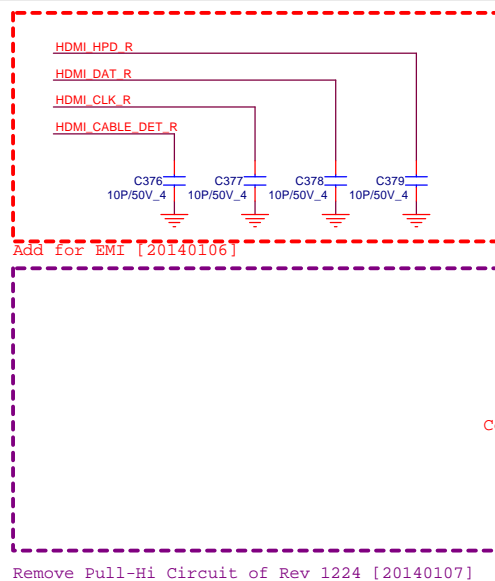


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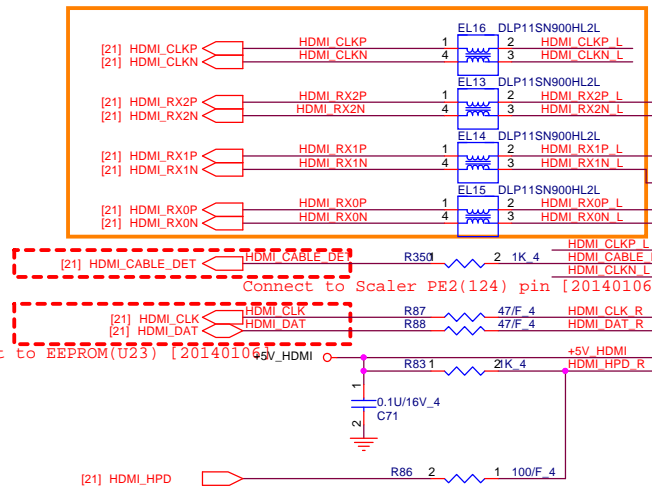
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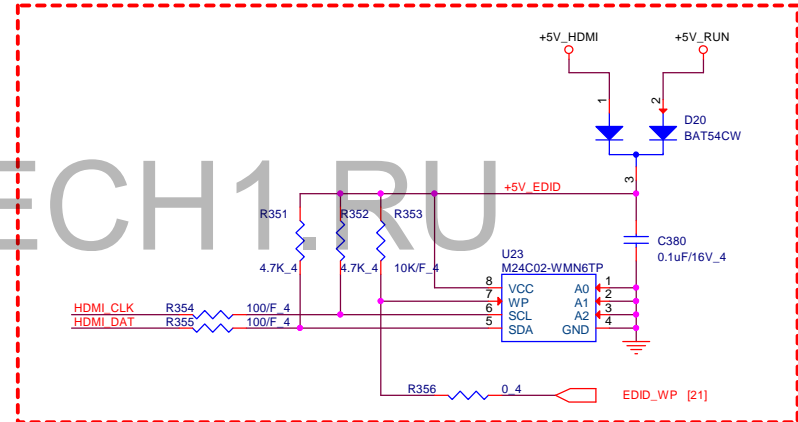
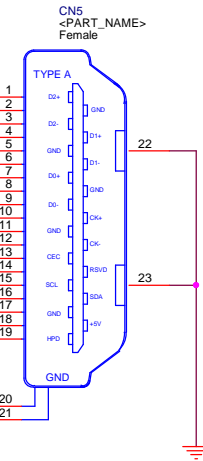




#EMI add choke

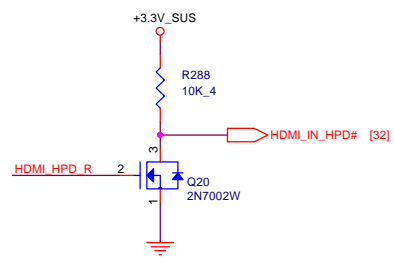


HDMI Conn.



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When HDMI IN ,inform to EC.



#Delete HDMI circiut

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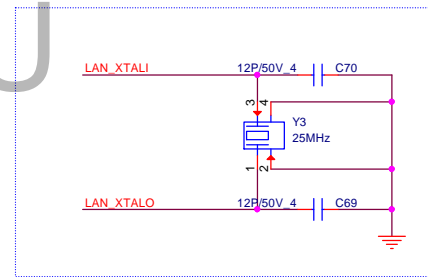
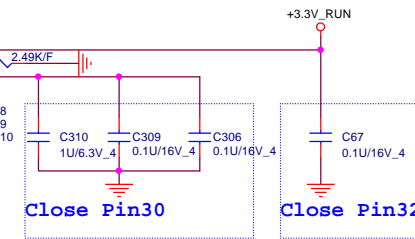
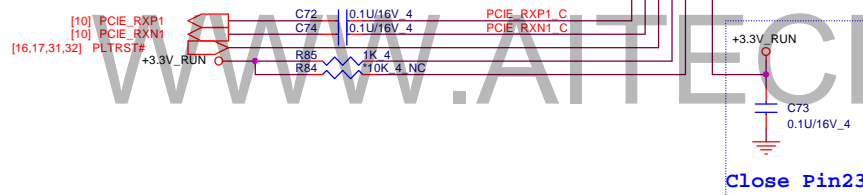
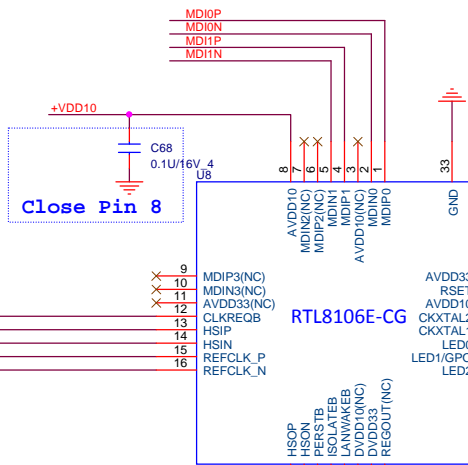
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PROJECT : QF2A ECO782413

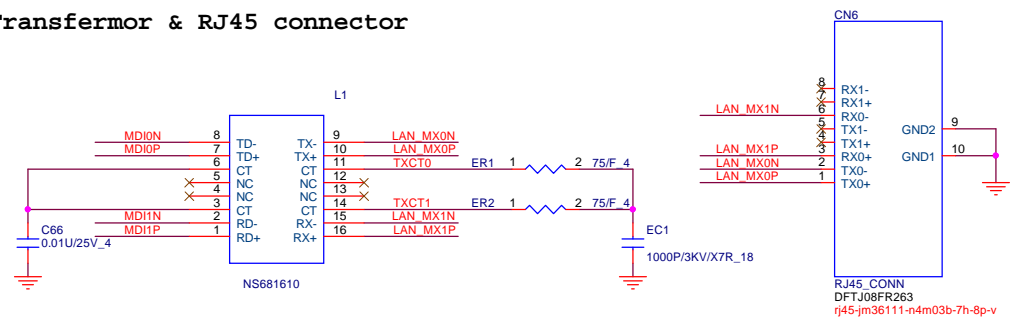
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CLKREQ: PU 1.8V_RUN at SOC side

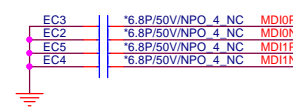
[10] PCIE_CLKREQ_LAN#
[10] PCIE_TXP1
[10] PCIE_TXN1
[11] CLK_PCIE_LANP
[11] CLK_PCIE_LANN



Transformer & RJ45 connector



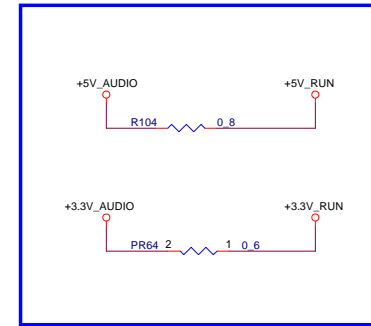
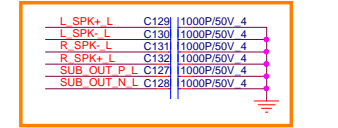
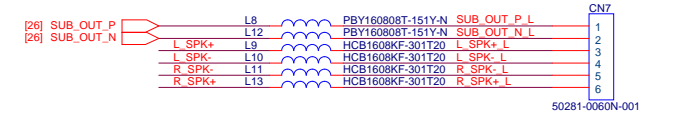
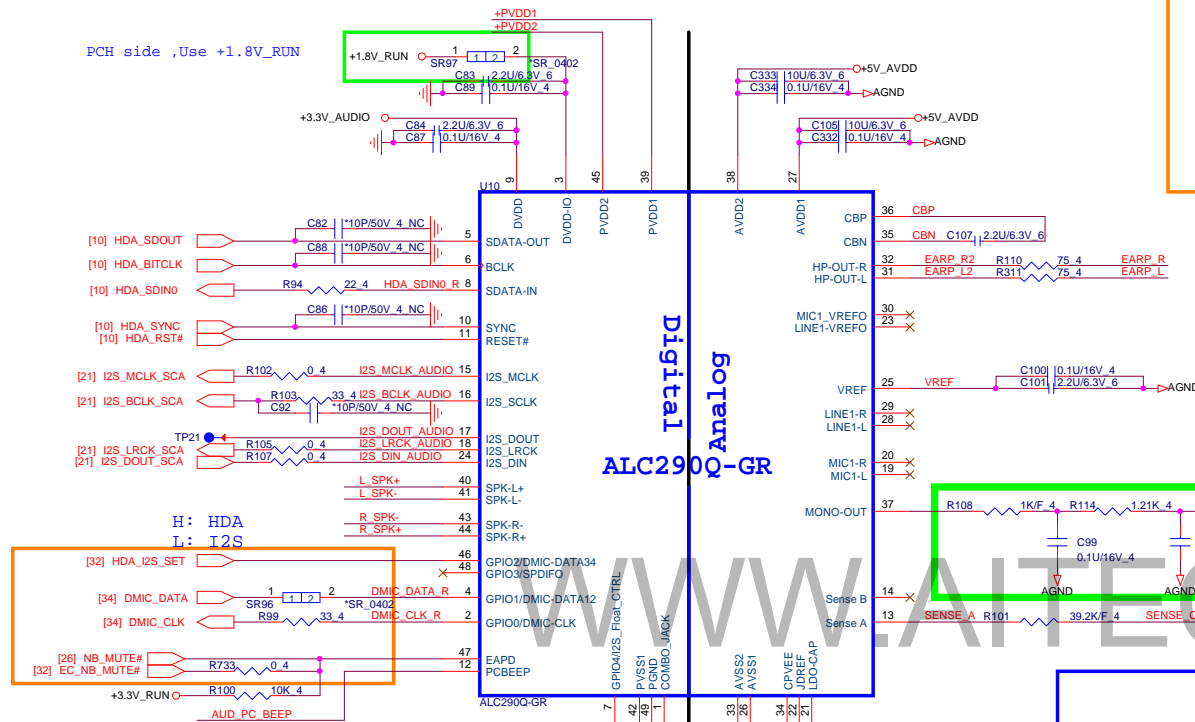
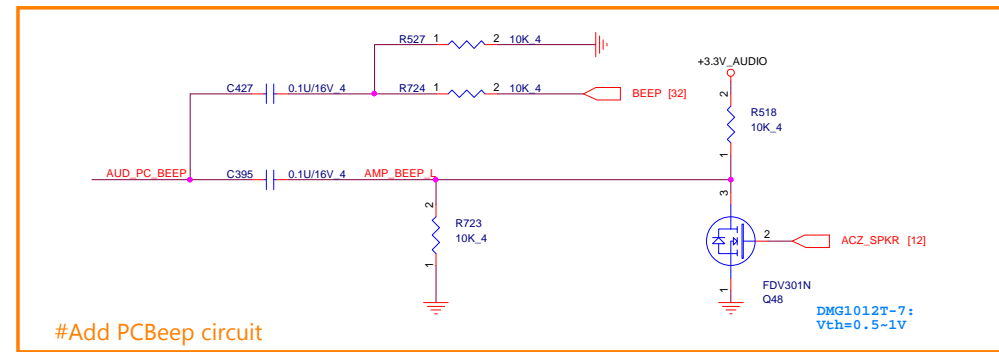
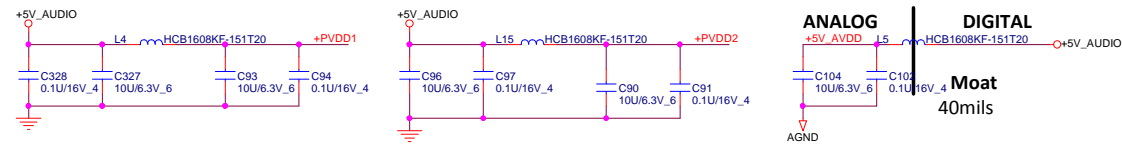
EMI



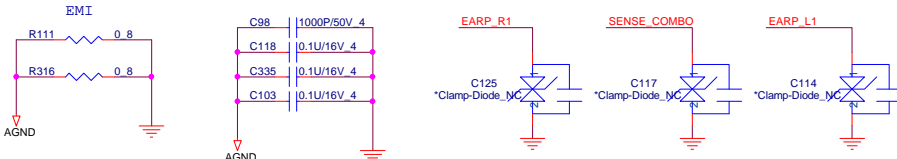
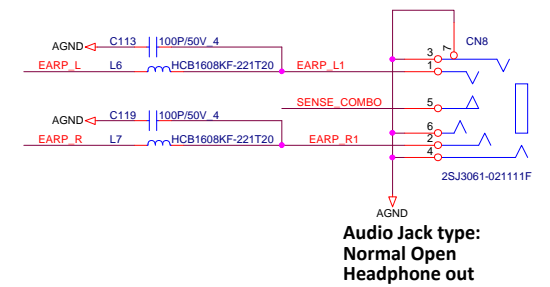
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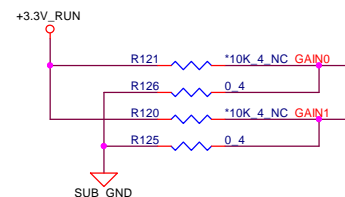
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Headphone Jack





Gain Setting Operation

GAIN1	GAIN0	Gain	Ri(Ω)
0	0	20dB	60k
0	1	26dB	30k
1	0	32dB	15k
1	1	36dB	9k

Table 1: The Gain Setting

$$f_{C(hipass)} = \frac{1}{2\pi R_i C_i}$$

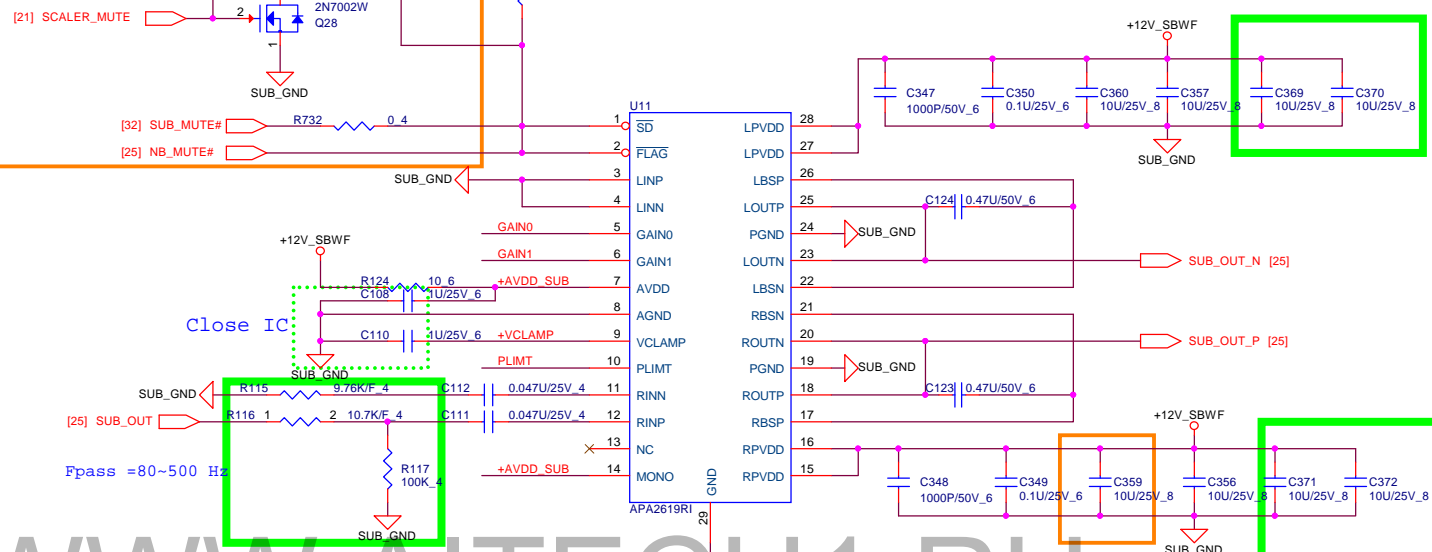
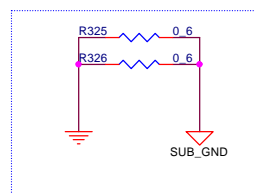
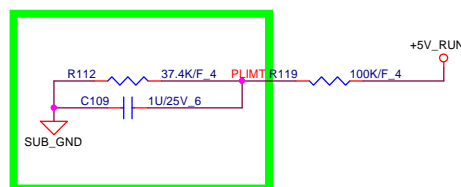
$$f_c = 1 / 2 \times 3.14 \times 60k \times 0.047u = 80 \text{ Hz}$$

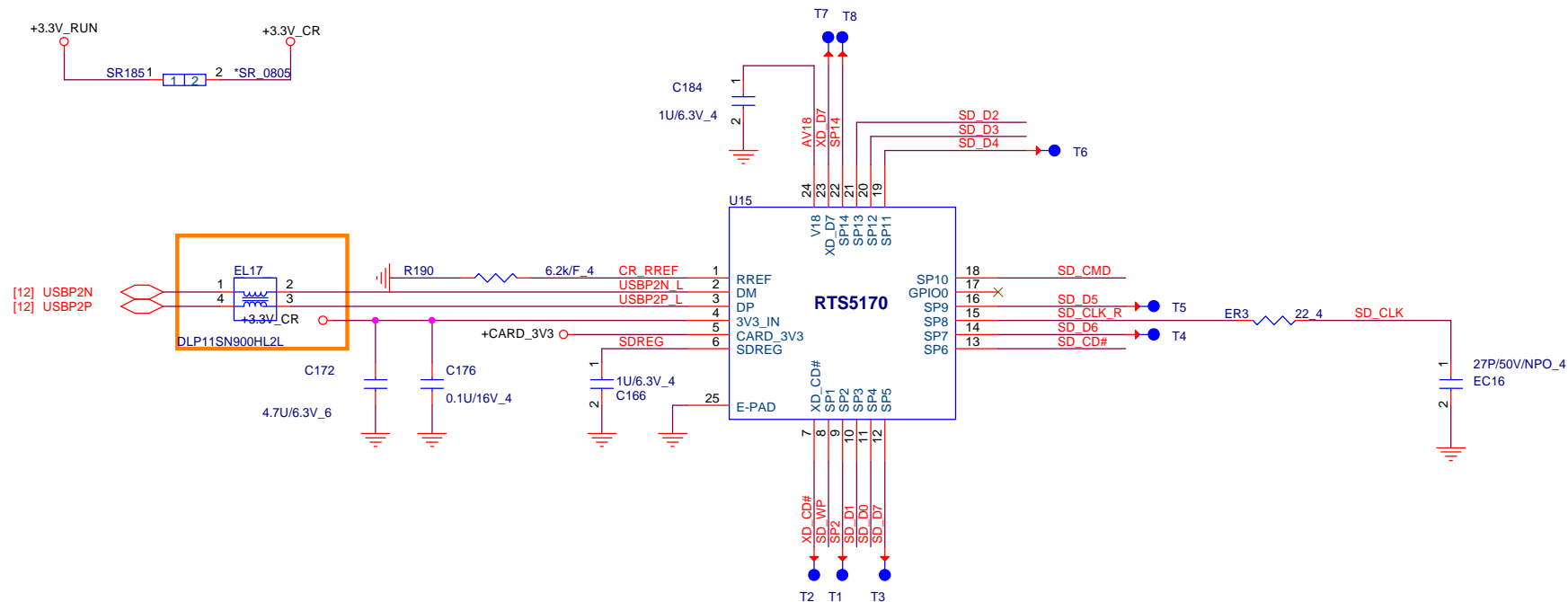
$$F_{pass} = 80 \sim 500 \text{ Hz}$$

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Test Conditions	PLIMIT Voltage	MAX Output Power @ THD+N=10%
PVDD=12V, Ri=8Ω	1.05V	2W
PVDD=12V, Ri=8 Ω	1.37V	3W
PVDD=12V, Ri=8 Ω	1.59V	4W
PVDD=12V, Ri=8 Ω	1.78V	5W
PVDD=12V, Ri=4 Ω	0.77V	2W
PVDD=12V, Ri=4 Ω	0.96V	3W
PVDD=12V, Ri=4 Ω	1.15V	4W
PVDD=12V, Ri=4 Ω	1.3V	5W

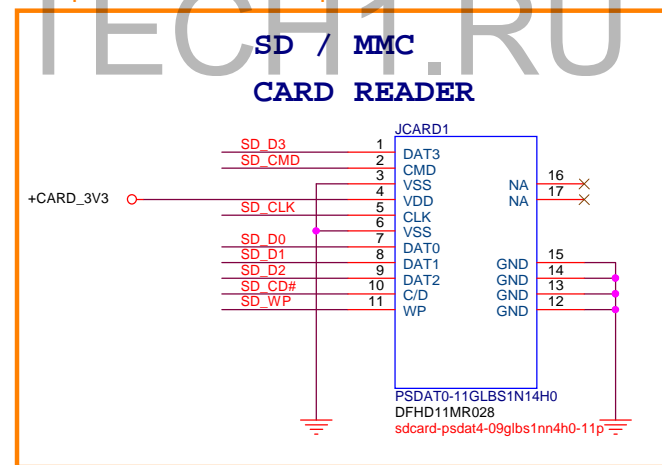
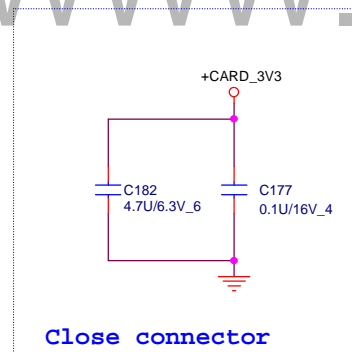
Table2. PLIMIT Typical Operation





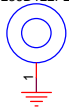
WWW.AITECH1.RU

#Update Conn & footprint

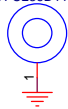


SCREW PAD

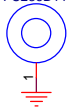
H5
H-C236D122P2



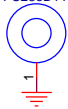
H6
*H-C236D110P2



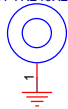
H7
*H-C236D110P2



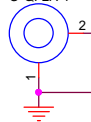
H9
*H-C236D110P2



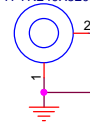
H10
*H-TR240X240BR240X240D110P1



H11
O-QF2A-1

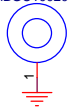


H12
*H-TR240X520BR240X520D110P2

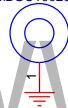


NUT

H1
MBGC1002010



H4
MBGC1002010



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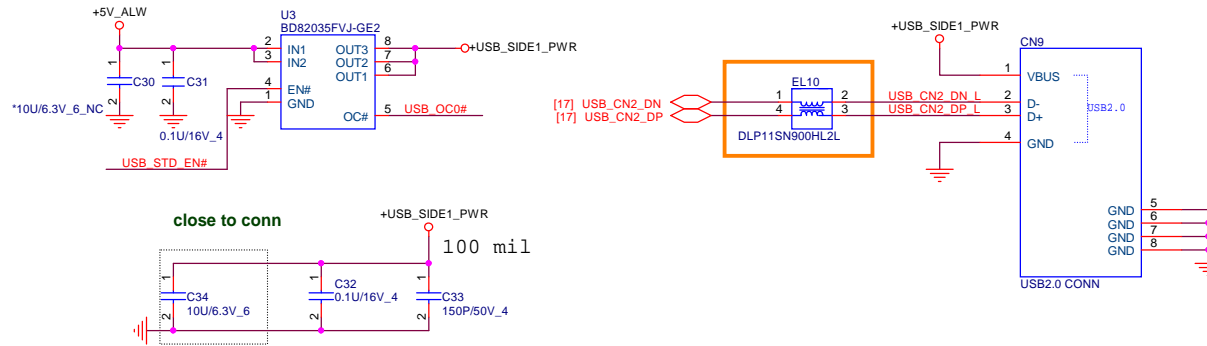
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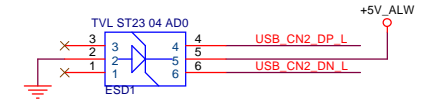
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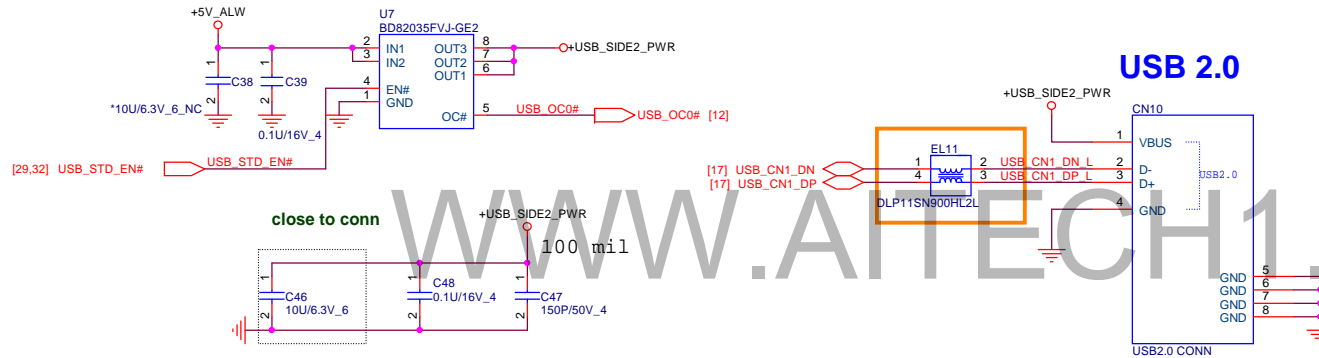
USB 2.0



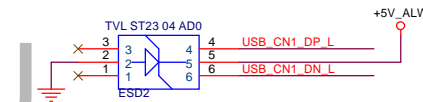
ESD Function
Place ESD diodes as close as USB connector.



USB 2.0

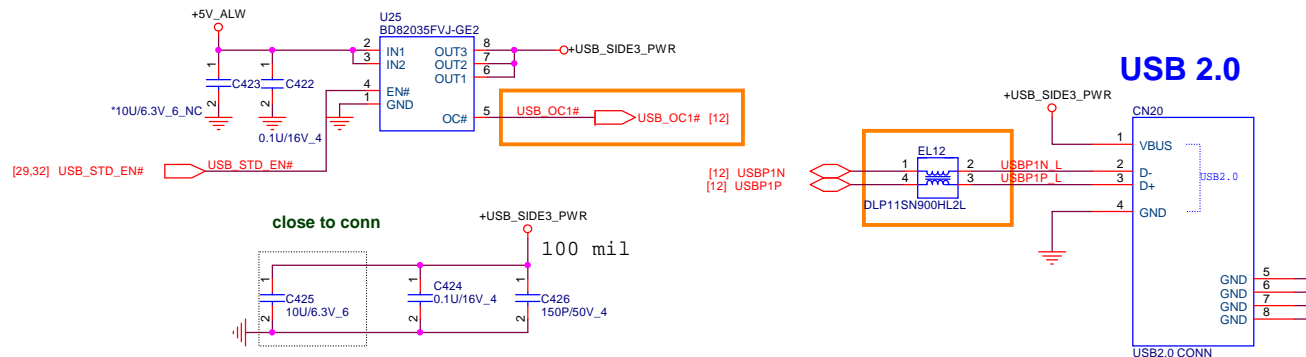


ESD Function
Place ESD diodes as close as USB connector.

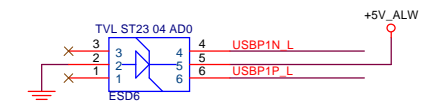


#Del Mini & Micro USB

USB 2.0



ESD Function
Place ESD diodes as close as USB connector.

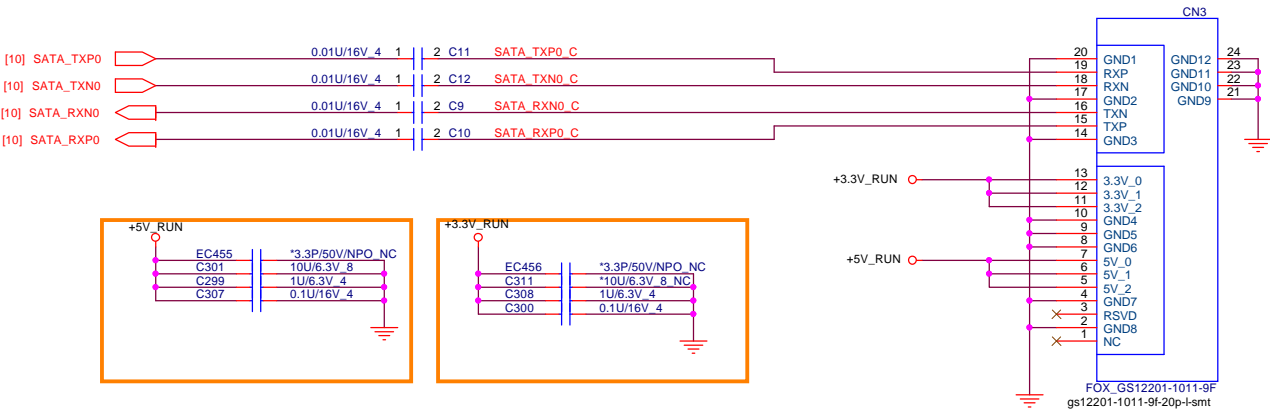


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HDD



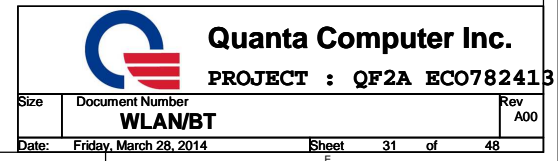
#Update Conn & footprint

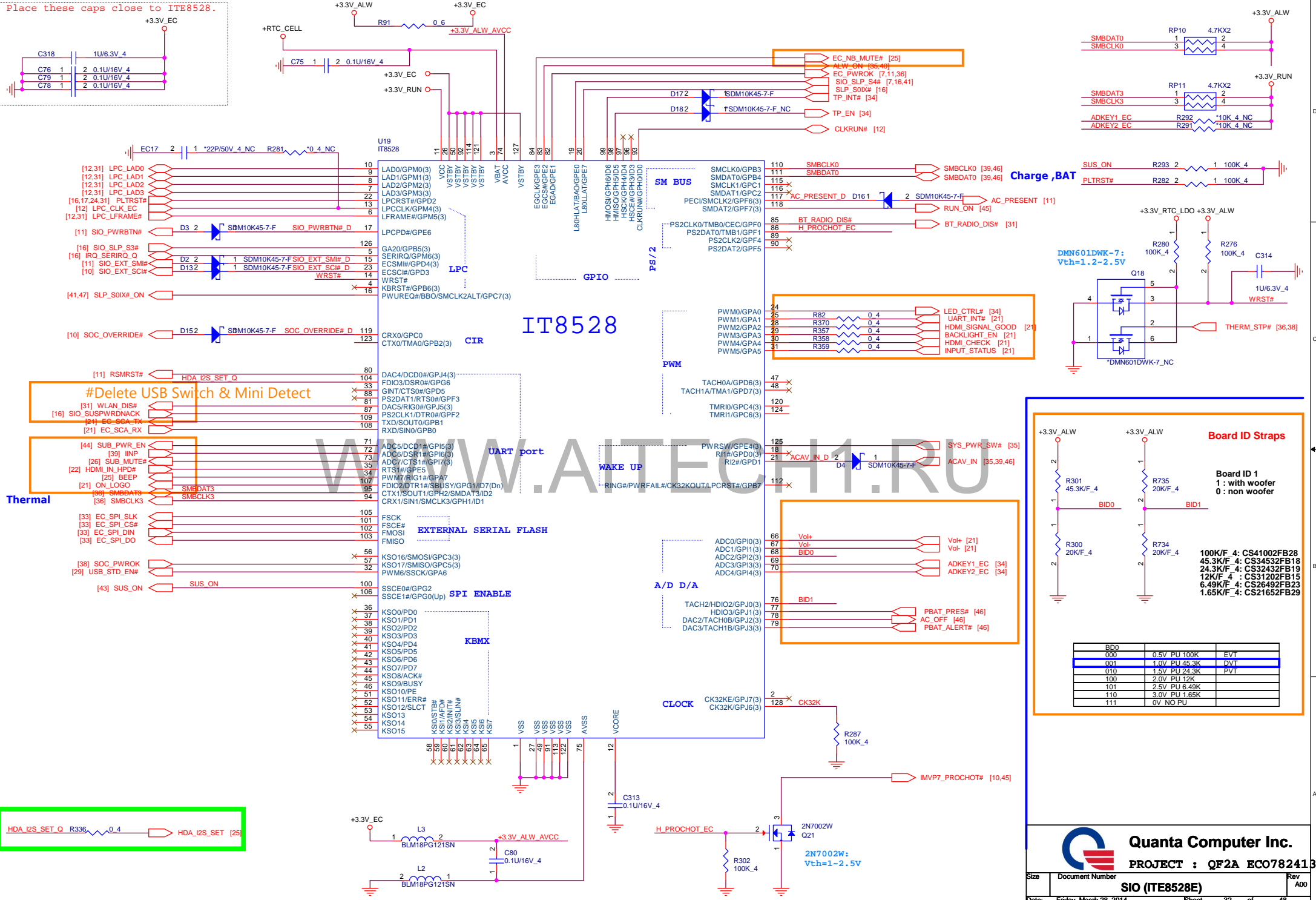


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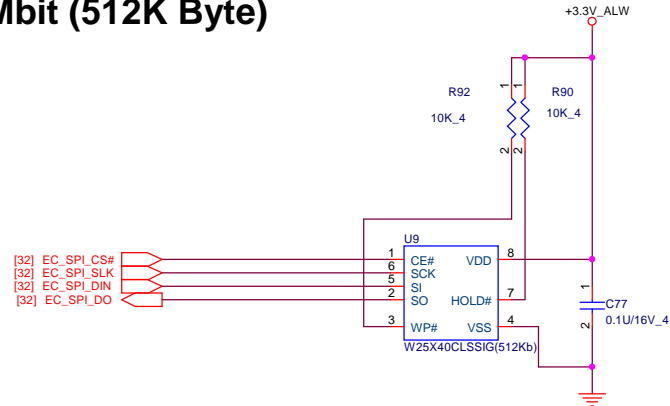
#Delete MSATA circiut

WWW.AITECH1.RU

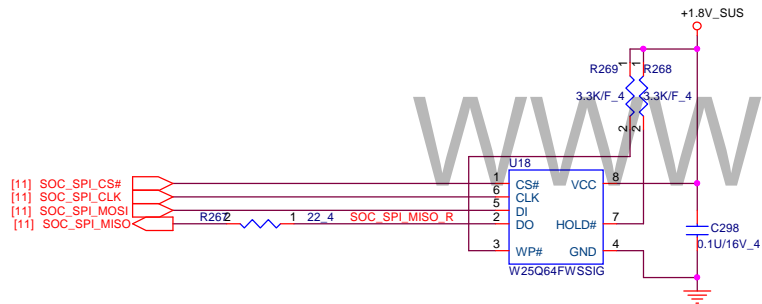




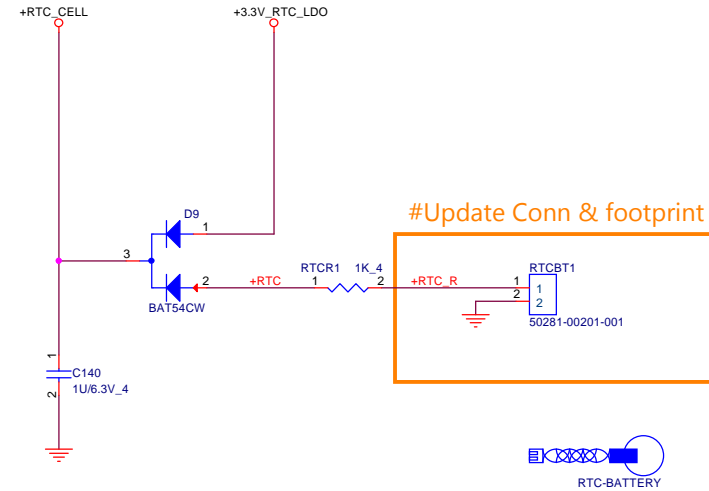
For EC 4Mbit (512K Byte)



For SOC 64Mbit (8M Byte)



RTC BATTERY



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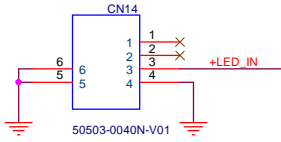
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FLASH / RTC		
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#Delete function Button

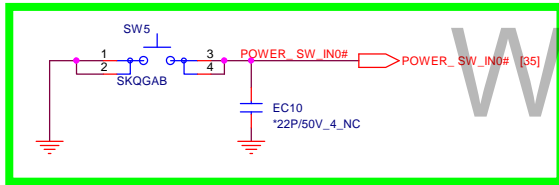
LED/IR CONN to LED/IR board

#Delete C359 & +3.3V_RUN for IR

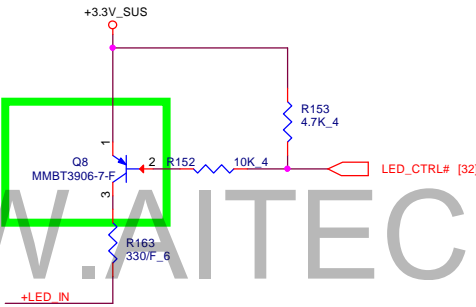


#Delete DBTV Conn

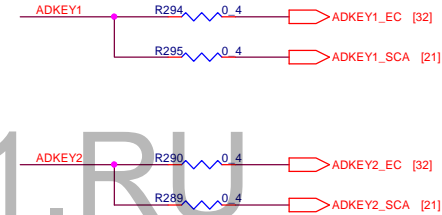
PWR BTN



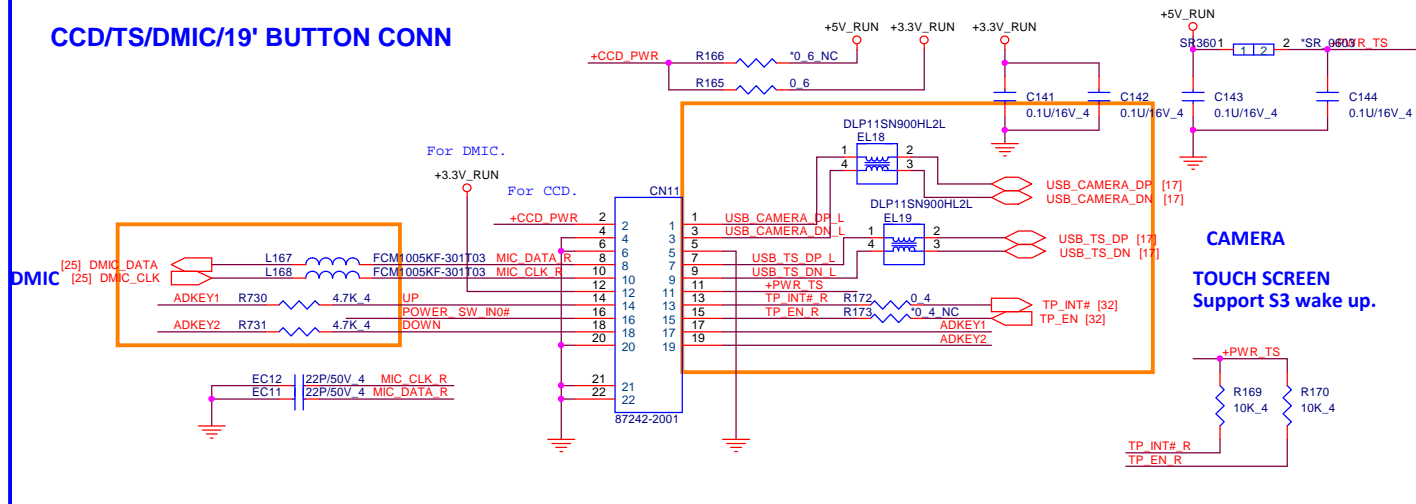
LED CONTROL



AD PIN Select



CCD/TS/DMIC/19' BUTTON CONN



CAMERA
TOUCH SCREEN
Support S3 wake up.

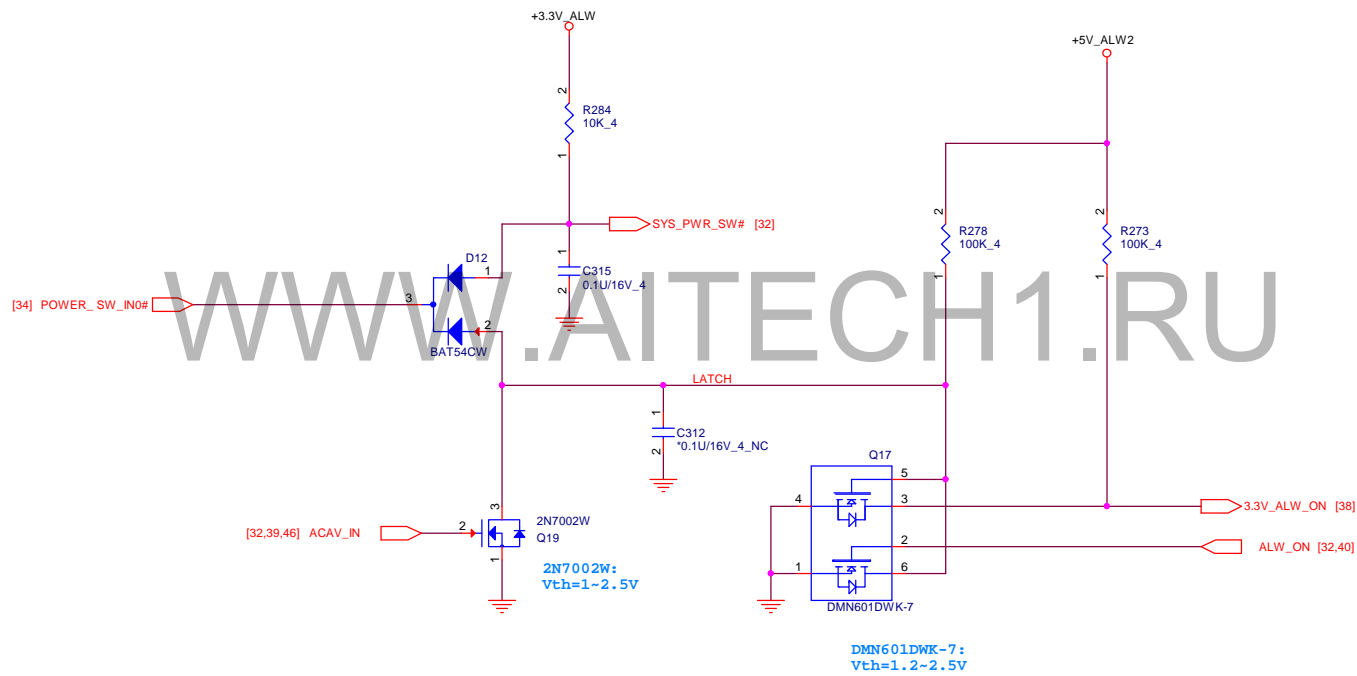


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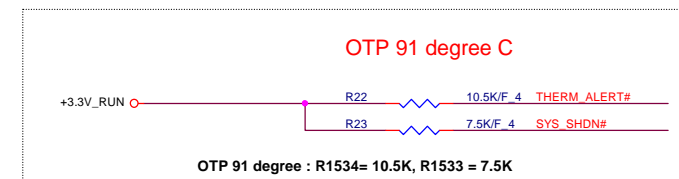
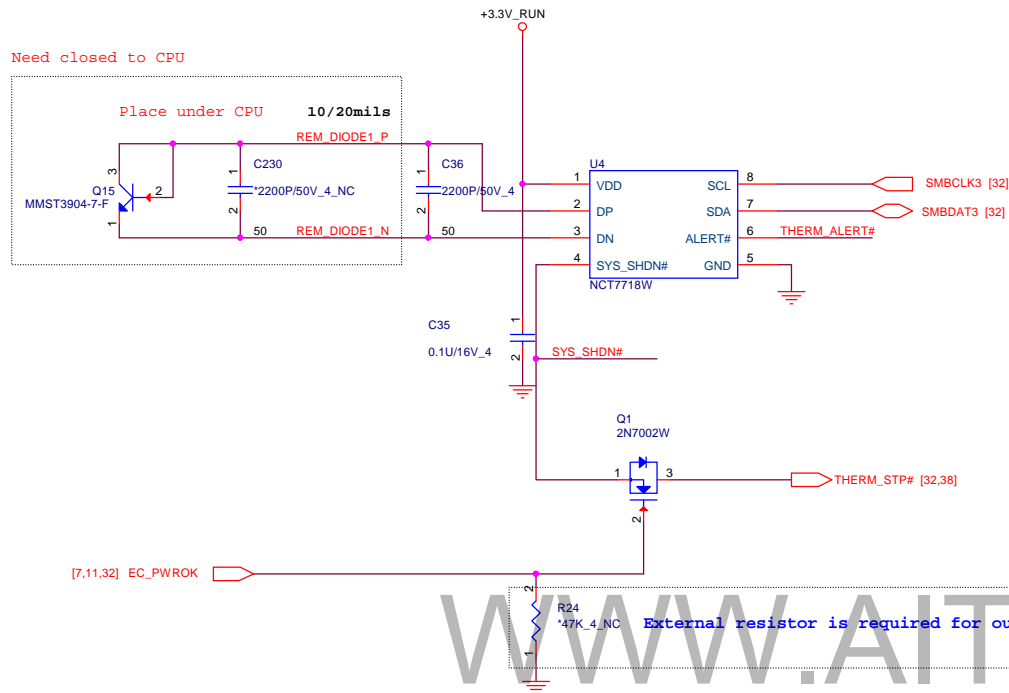
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3VALW ON POWER LOGIC



THERMAL IC



SYS_SHDN#	2K	7.5K	10.5K	14K	18.7K
ALERT#					
2K	77 °C	87 °C	97 °C	107 °C	117 °C
7.5K	79 °C	89 °C	99 °C	109 °C	119 °C
10.5K	81 °C	91 °C	101 °C	111 °C	121 °C
14K	83 °C	93 °C	103 °C	113 °C	123 °C
18.7K	85 °C	95 °C	105 °C	115 °C	125 °C



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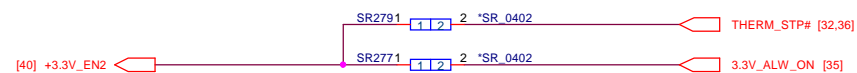
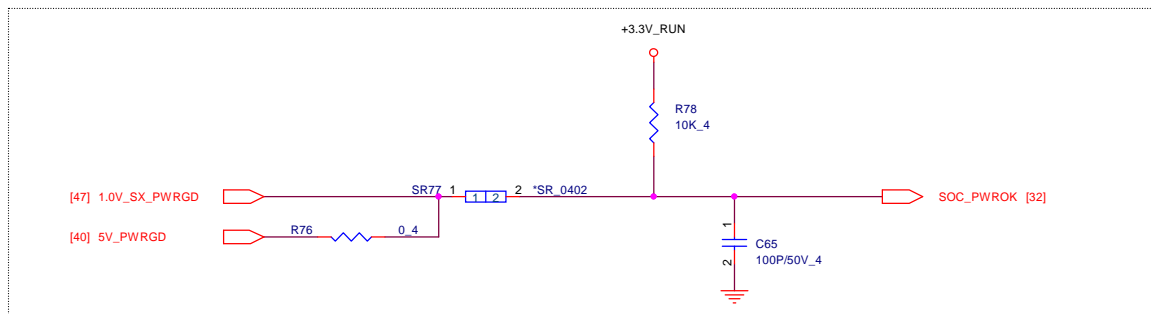
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	Blank	A00
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WWW.AITECH1.RU

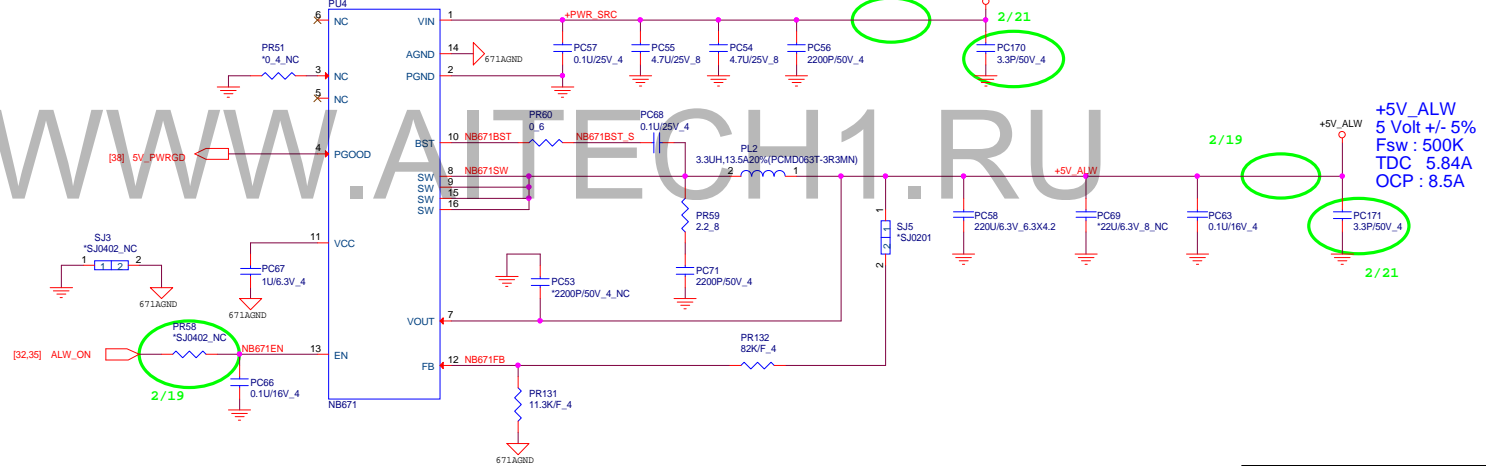
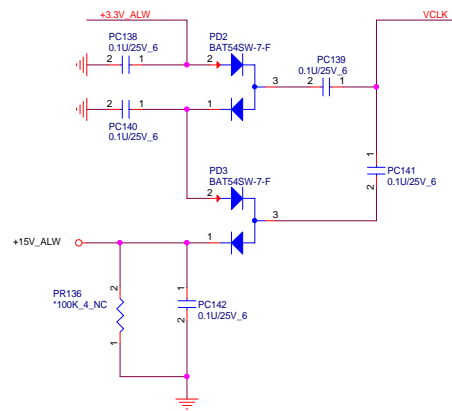
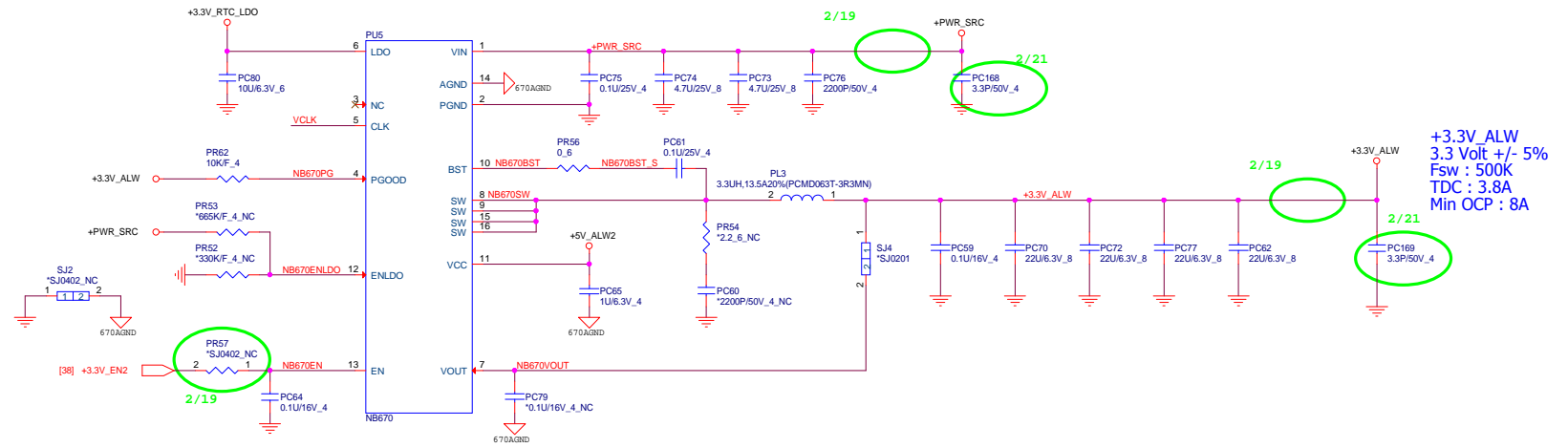


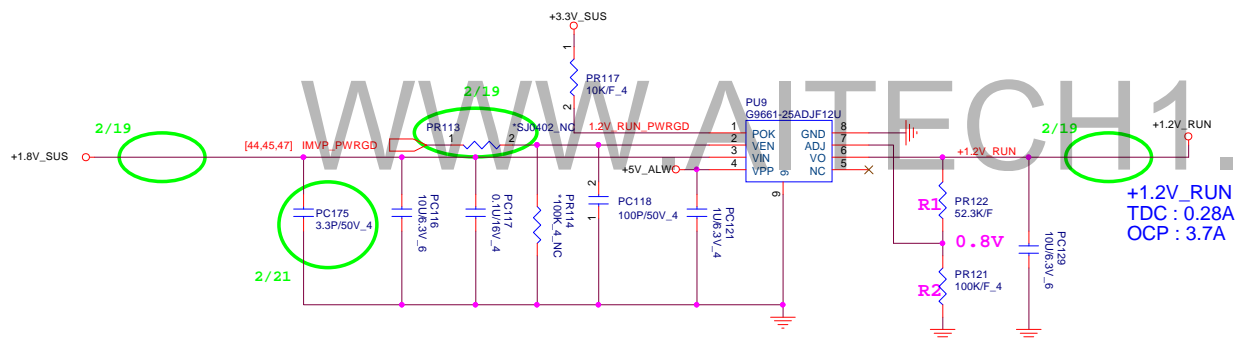
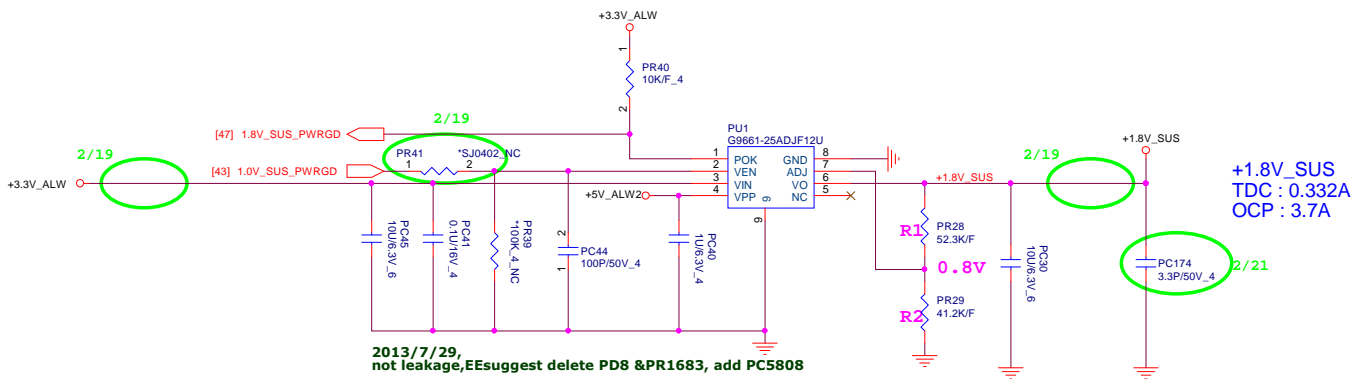
Quanta Computer Inc.

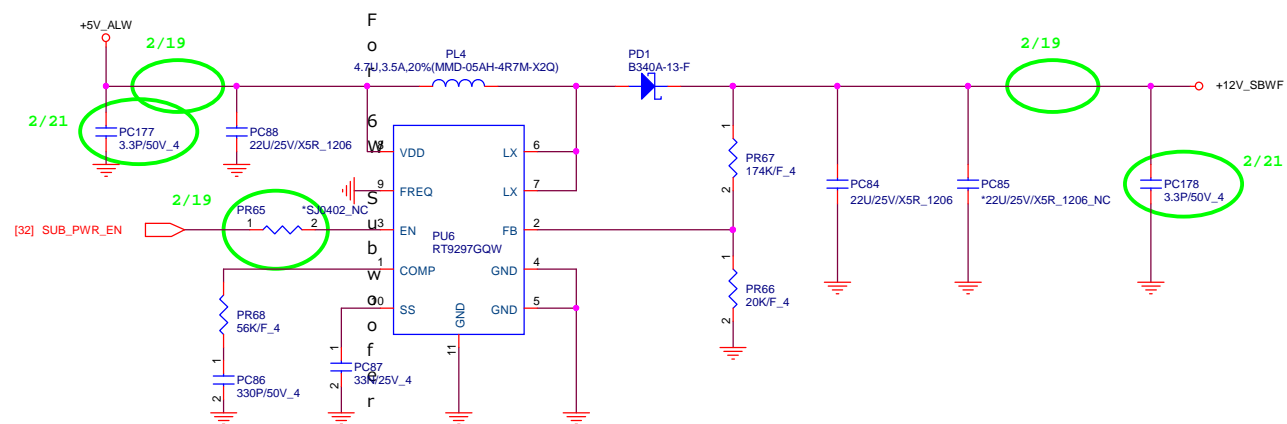
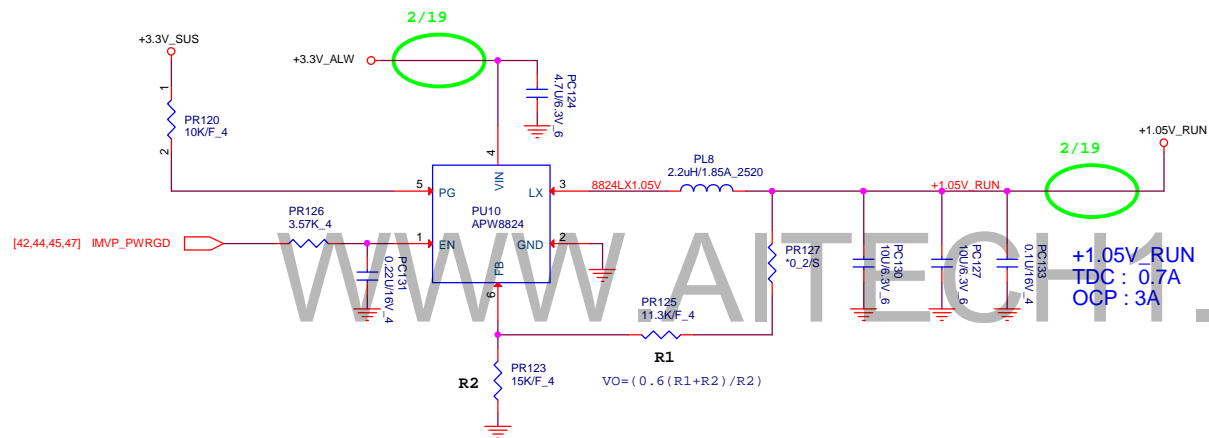
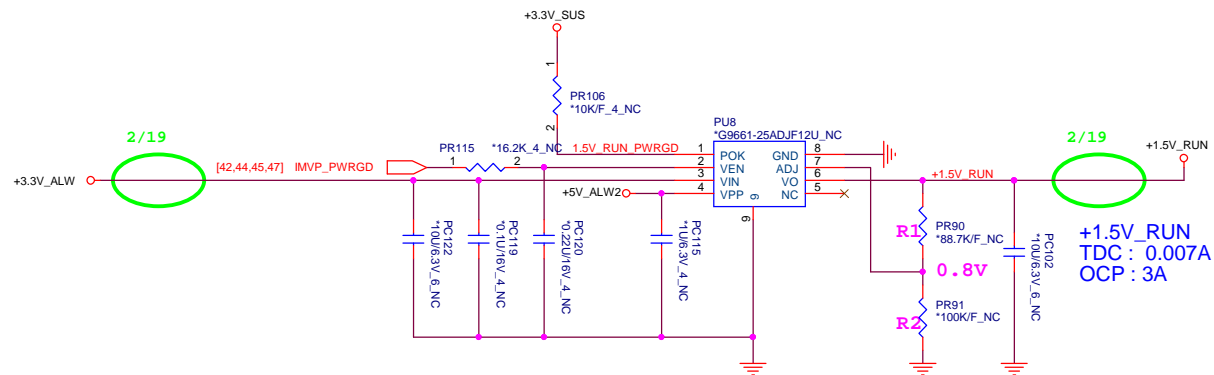
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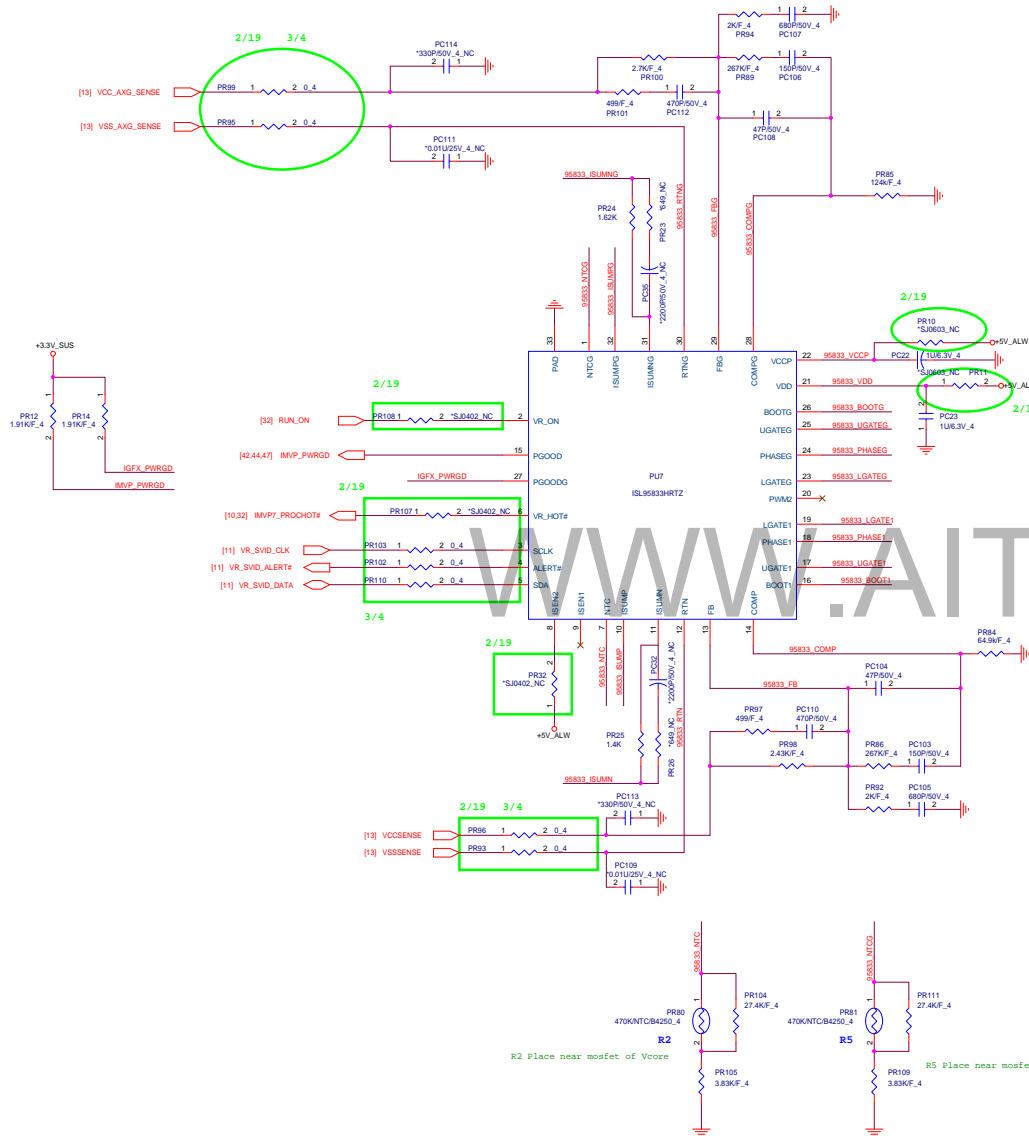
System Reset Circuit

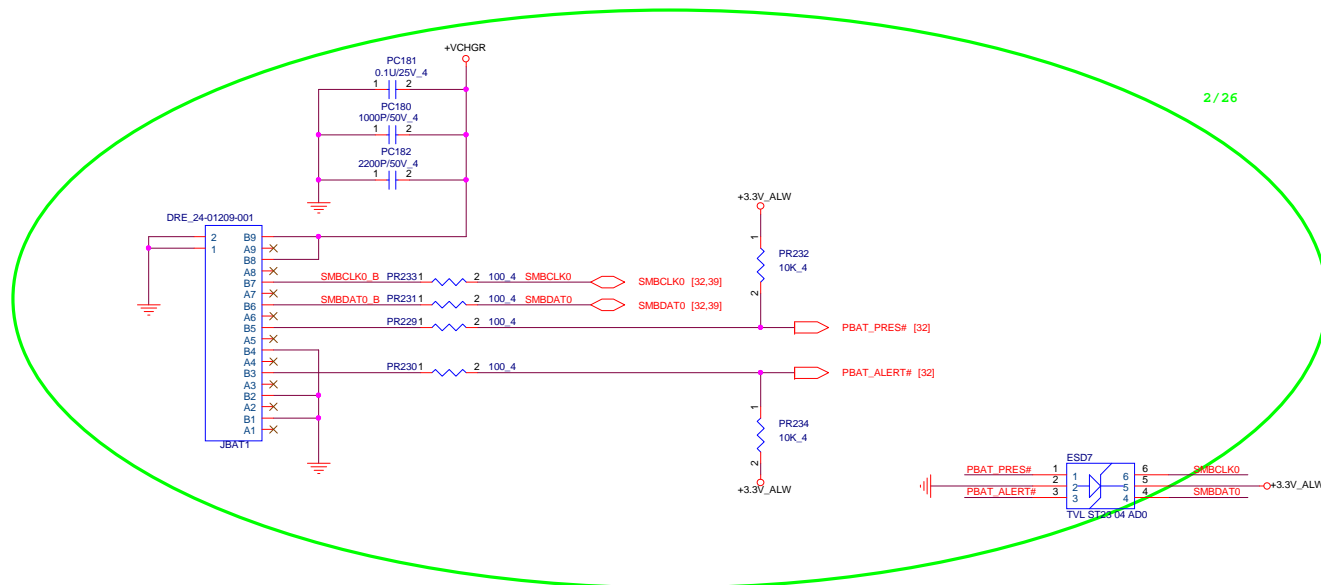




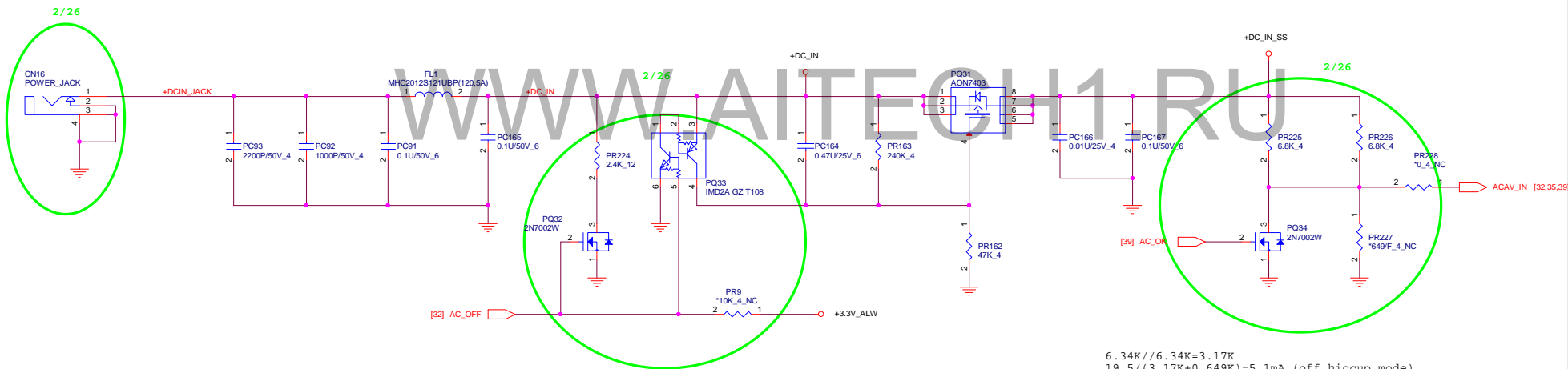


12V/500mA (6W)
Frequency: 640KHz





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$6.34K / 6.34K = 3.17K$
 $19.5 / (3.17K + 0.649K) = 5.1mA$ (off hiccup mode)
 $(5.1m \times 5.1m \times 3.17K) / 2 = 0.041W$ (<0.0625W, 0402 size)
 $5.1m \times 5.1m \times 0.649K = 0.0168W$ (<0.0625W, 0402 size)

	NO Battery sku	Battery sku
PR225	6.34K(CS26342FB27)	6.8K(CS26802JB11)
PQ34	NC	2N7002W(BAM70020004)
PR226	6.34K(CS26342FB27)	6.8K(CS26802JB11)
PR227	649(CS16492FB13)	NC
PR228	0(CS00002JB38)	NC

